An Improved Low Phase Noise *LC*-VCO with Wide Frequency Tuning Range Used in CPPLL

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Abstract: Based on TSMC 0.18μm CMOS process, a complementary cross-coupled differential *LC* voltage controlled oscillator (*LC*-VCO) used in charge pump phase-locked loop (CPPLL) frequency synthesizer for satellite receiver with low phase noise and wide frequency tuning range is designed and implemented. The VCO adopts self-bias structure to remove flicker noise produced by tail current. Programmable *LC* tanks are introduced at the common source of cross-couple transistors to eliminate second harmonics of resonant frequency. Distributed biasing is applied for a wider linear tuning range. An optimized switch is proposed to lower on-resistance. The measured results show that the VCO exhibits a 53.8% tuning range from 1.02GHz to 1.77GHz. From the carrier frequency of 1.4 GHz, the phase noise of the VCO can reach -131.2 dBc/Hz at 1MHz offset. The core circuit consumes 7.7mA with 1.8V supply voltage.

Keywords: low phase noise, wide tuning range, distributed biasing, optimized switch

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1. Introduction

Frequency modulation is widely used in communication system especially for long distance communication. A wide utilization of frequency synthesizer in the RF system makes it possible to generate an accurate frequency signal for frequency modulation [1]. In the RF system, noise produced by frequency synthesizer directly deteriorates the overall noise performance of the system [2]. Meanwhile, the VCO is one of the major contributors of the out-of-band noise in a PLL frequency synthesizer [3]. Thus, to design a low phase noise VCO is necessary and significant for a high performance communication system, which is a challenge for us in consideration of tuning range, power consumption and other characteristics.

With a mature understanding of phase noise mechanism [4]-[6], many attempts to optimize phase noise of VCO have been made in recent years. In Reference [7], switchable cross-coupled pairs are used for lower transconductance and thereby improve $1/f^3$ noise. However, as a result, the complexity of the timing logic is inevitably increased. In order to prevent the *Q*-factor degradation of resonant tanks in VCO, MOS switches featuring high off-on resistance ratio (R_{OFF}/R_{ON}) are used, and transistors with large gate width are introduced to achieve a sufficiently low R_{ON}. However, the C_{OFF} associated with such wide transistors will cause serious performance degradation[8], [9].

This paper introduce how VCO contribute phase noise to CPPLL, presents a complementary cross-coupled differential *LC*-VCO that can achieve low phase noise and large frequency tuning range. Self-bias structure is applied to remove flicker noise produced by tail current. Programmable *LC* tanks are introduced at the source of cross-coupled transistors to eliminate second harmonics of resonant frequency. Distributed biasing is adopted to widen the linear tuning range of every selected band. The switches used in the design have been optimized to enhance the *Q*-factor. The presented VCO is fabricated using

TSMC 0.18μm CMOS technology, measurement of which is performed for validation.

2. CPPLL noise analysis

We choose CPPLL rather than others for its stability and larger acquisition range. A brief block diagram of the CPPLL is shown in Fig.1. Phase/frequency detectors (PFD) sense phase and frequency
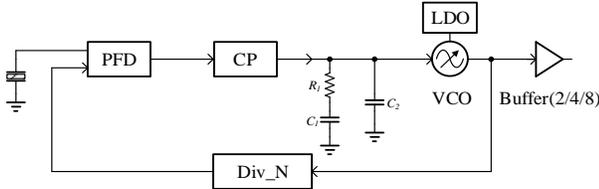

Fig.1. CPPLL block diagram.

differences between reference clock signal and output of divider. Charge pump sinks or sources current for a limited period of time according to the voltage produced by the previous PFD. The loop filter (consisting of R_1, C_1 and C_2) following CP produces voltage which controls VCO. The low dropout regulator (LDO) supplies for the VCO. The frequency divider (FD) between VCO output and PFD input makes a feed-back loop to ensure that output signal frequency is independent of process, supply voltage, temperature and other interferences. To formulate the CPPLL output phase noise contributed by VCO, we need to derive the transfer function from the VCO phase to the CPPLL output phase. Although CPPLL is a nonlinear system, in the vicinity of lock state we can make a linear approximation in phase domain for intuitive understanding. A linear model is constructed in Fig.
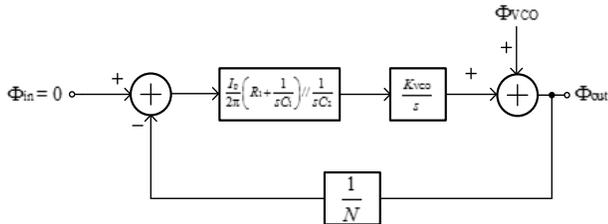

Fig.2. Phase-domain linear model for deriving VCO's effect on CPPLL phase noise

2, where $\frac{I_p}{2\pi}\left(R_1+\frac{1}{sC_1}\right)//\frac{1}{sC_2}$, $\frac{K_{VCO}}{s}$ and $\frac{1}{N}$ represent CP, VCO and FD respectively.

In order to analyze VCO's effect, we make $\Phi_{in}=0$ to signify that reference clock signal is noiseless. Starting from the output, we have:

$$-\frac{\phi_{out}}{N}[\frac{I_p}{2\pi}\left(R_1+\frac{1}{sC_1}\right)//\frac{1}{sC_2}]\cdot\frac{K_{VCO}}{s}+\phi_{VCO}=\phi_{out} \tag{1}$$

Equation （1） allows us to derive phase transfer function from VCO to PLL output as :

$$\frac{\phi_{out}}{\phi_{VCO}}(s)=\frac{s^3+\frac{C_1+C_2}{R_1C_1C_2}\cdot s^2}{s^3+\frac{C_1+C_2}{R_1C_1C_2}\cdot s^2+\frac{1}{N}\cdot\frac{I_pK_{VCO}}{2\pi C_2}\cdot s+\frac{1}{N}\cdot\frac{I_pK_{VCO}}{2\pi R_1C_1C_2}} \tag{2}$$

The transfer function contains two zeros at the origin and one zero near origin, three poles on the right of the zeros, exhibiting a high-pass behavior. The VCO phase noise is shaped by the transfer function. It can be proved that the phase noise out of loop bandwidth follows VCO's phase noise [3].
Taking other noise sources (reference clock, PFD, CP, FD and etc.) into consideration, we can make a conclusion that PLL's output phase noise measured at high offset frequencies is worse than VCO's.

3. Circuit Design

The theories to derive the phase noise of VCO have been researched for many years. The theory proposed by Ali Hajimiri [6], which can make an accurate, quantitative prediction about the phase noise is described in equation (3):

$$L\{\Delta\omega\}=10\cdot\lg(\frac{c_o^2}{q^2_{max}}\cdot\frac{\overline{i_n^2}/\Delta f}{8\cdot\Delta\omega^2}\cdot\frac{\omega_{1/f}}{\Delta\omega})+10\cdot\lg[\frac{1}{2}\cdot\frac{kT}{V^2_{max}}\cdot\frac{1}{R_p\cdot(C\omega_o)^2}\cdot(\frac{\omega_o}{\Delta\omega})^2] \tag{3}$$

Where ω_O is the carrier frequency, $\Delta\omega$ is the offset frequency from ω_O, R_p is equivalent parallel resistance, k is Boltzmann's constant, V_{max} is the voltage swing across the tank, T is the temperature, q_{max} is the maximum charge displacement across the capacitor, c_0 is the weight of low-frequency noise, $\overline{i_n^2}/\Delta f$ is the white power spectral density, and $\omega_{1/f}$ is 1/f-noise corner frequency. The first item in equation (3) accounts for phase noise in the $1/f^3$ portion while

the second item accounts for the phase noise in the $1/f^2$ portion.

In the vicinity of resonance frequency, the Q-factor of the LC tank is expressed as equation (4):

$$Q = \frac{R_p}{\omega_O L} = \omega_O R_p C = Q_L // Q_c \qquad (4)$$

So, the equation (3) can be modified as:

$$L\{\Delta\omega\} = 10 \cdot \lg(\frac{c_O^2}{q^2_{max}} \cdot \frac{\overline{i_n^2}/\Delta f}{8 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}) + 10 \cdot \lg[\frac{1}{2} \cdot \frac{kT}{V^2_{max}} \cdot \frac{1}{QC\omega_O} \cdot (\frac{\omega_O}{\Delta\omega})^2] \qquad (5)$$

In this design, guided by equation (5), the LC-VCO with optimized phase noise is presented, the core schematic of which is shown in Fig. 3.
There is no current source in the schematic, so the flicker noise due to current source can be removed totally. A complementary cross-coupled structure is adopted rather than only a cross-coupled structure because the structure can produce twice the voltage swing for a given current and inductor design, which can reduce phase noise according to equation (3). The direct-current operating points are determined by diode-connected MOS transistors between power and ground provided by LDO which can reduce VCO's sensitivity to supply voltage. MOS
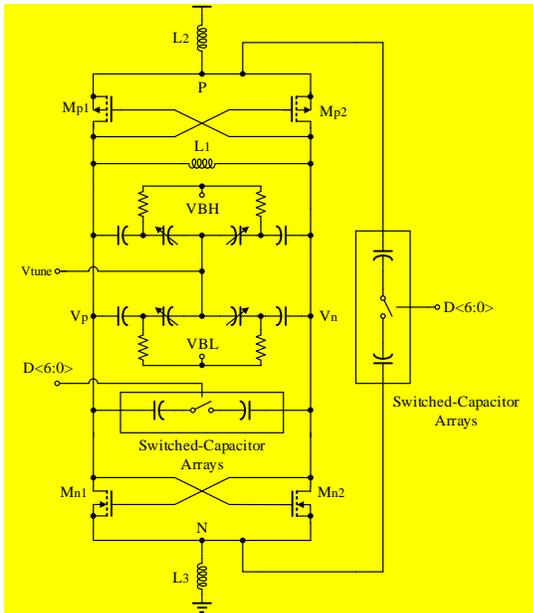
Fig.3. The proposed VCO core schematic.

transistors here are used to work as negative resistor,

cancelling loss in the LC tank due to parasitic resistance of inductor, capacitor and others. In this design, the parameters of PMOS and NMOS are set to produced symmetric output swing by simulation iteration operation for a given frequency range, which benefits phase noise optimization [8]. The parameter of main components in VCO is shown in Table I.

Table I Parameters of main components in VCO

Components	Parameter	Value
L_1	Inductance[nH]	2.95
$L_2(L_2)$	Inductance[nH]	1.69
$Mn_1(Mn_2)$	W/L[μm/μm]	32*(2/0.2)
$Mp_1(Mp_2)$	W/L[μm/μm]	32*(6/0.2)

There are two 7-bit binary-weighted switched capacitor arrays controlled by the same digital codes, D<6:0>, in the proposed topology. For a compromise of the linearity and layout area, the codes are implemented with a segmented architecture, in which the 2 LSBs are implemented using a binary architecture while the 5 MSBs are implemented in a unary way. The capacitor array in parallel with L_1 is proposed to extend the tuning range instead of increasing VCO gain, which can realize coarse tuning. The other connected between nodes P and N is in parallel with L_2 and L_3, whose purpose is to compose a narrow band circuit for resonance at second harmonic, preventing the degradation of the Q-factor of the tank when the transistors operate in the triode region[11]. We choose programmable switched capacitors between nodes P and N rather than a fixed capacitor because we can choose appropriate resonant frequency according to the band selection.

In order to perform the fine tuning of VCO with a wide linear range, distributed MOS varactor biasing is applied[12].The varactor we used in the design is accumulation-mode MOS varactor, which is shown in Fig. 4 (a). This structure is obtained by placing an NMOS transistor inside an n-well. If $V_G < V_S$, then electrons in the n-well are repelled from silicon/oxide interface and a depletion region is formed. Under this condition, the capacitance seen from the gate is given by the series combination of the oxide and depletion capacitance. As V_G exceeds

V_S, the interface attracts electrons from the n^+ source/drain terminals, creating a conduction channel. As a result, the total capacitance seen from the gate rises to that of the oxide. The C/V characteristics of the varactor is shown in Fig. 4 (b). The linear range of the structure is limited. To solve this problem, we shunt two varactors in parallel with two different voltage bias, VBH and VBL, which is shown in Fig.3. The C/V characteristics of distributed biasing varactors is shown in Fig.5. Compared to the conventional structure whose varactor is biased by a single reference voltage, this design can achieve almost twice linear range. As a consequence, we can enlarge tuning range of every selected band and reduce the VCO gain for a given frequency range, which makes a good trade-off between phase noise and tuning range.

(a) (b)
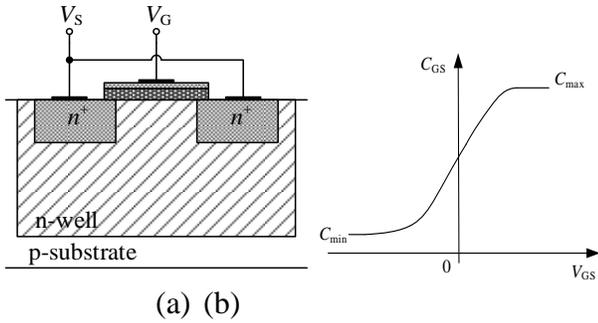
Fig.4. (a) MOS varactor , (b) resulting C/V characteristic of the varactor
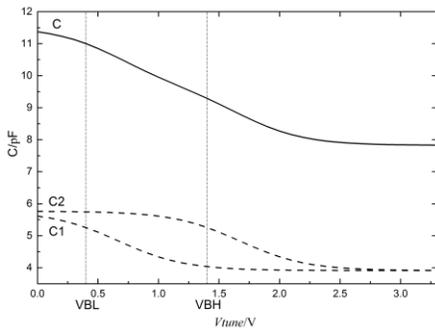
Fig.5. C/V characteristic of the varactors with distributed biasing

Another issue should be paid attention to is the design of the switch used in capacitor arrays, which concerns the Q-factor of the LC tank. We hope the switch is ideal, but the parasitic effect and voltage swing between the switch make it hard to implement an ideal switch. There is a trade-off in the design of

switch size. To realize high quality of capacitor when the switch is on, we need large size switch to minimize the on-resistance. To minimize parasitic capacitance of the switch when the switch is off, we need to design small size switch MOS transistor to degrade C_{gs} and C_{gd}. A conventional structure is shown in Fig.6 (a), where the on-resistance is introduced by MOS switch. Ideally, the switch transistor is in deep triode region when the switch is on. The resistor is equal to

$$R_{on} = \frac{1}{\mu_n C_{ox} \dfrac{W}{L} (V_{GS} - V_{TH})} \qquad (6)$$

However, the voltage swing appearing at source of the MOS switch may drive it out of the region. As a result, the on-resistance varies along with the output voltage swing of the VCO, which will deteriorate the phase noise of the VCO. To solve the problem, an optimized structure is used in this design as described in Fig.6(b). Since the structure is symmetrical with differential voltage swing, node A is ac ground here. When the switch is on, the common source of the two transistor experiences little voltage swing and the on-resistance almost keeps a constant consequently. Additionally, when the switch is off, the optimized structure is switched off more thoroughly and introduces almost half parasitic capacitance if the switch sizes are equal in the two structures.


(a) (b)
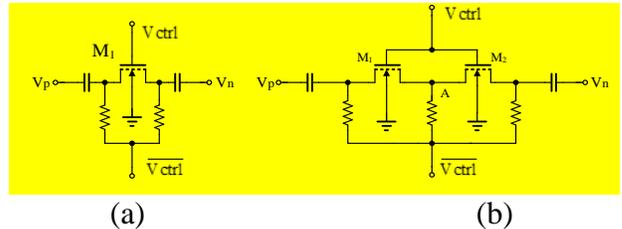
Fig.6. (a) a conventional switch (b) an optimized switch

4. Implementation and Measurements

This proposed low phase noise VCO is integrated in a receiver which is fabricated using TSMC 0.18μm CMOS technology. In our frequency synthesizer, the

VCO output is divided by a divide-by-2 quadrature frequency divider to generate quadrature local oscillating (LO) signal for quadrature down conversion. After the divider, an output buffer is adopted for testing. According to the system requirement, the loop bandwidth of the frequency synthesizer is set to 100 kHz. Fig. 7 shows a micrograph of the proposed VCO, occupying an area of $820*1080\mu m^2$.
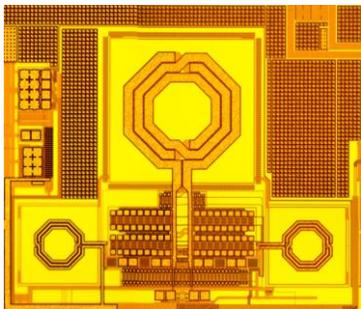

Fig.7.Micrograph of proposed VCO.

An Agilent E5052B signal source analyzer is used to measure the synthesizer parameters in the test. The f-V tuning characteristic of the VCO is shown in Fig. 9(a). The VCO achieves a tuning range of 53.8% from 1.02 GHz to 1.77 GHz. Fig. 9(b) shows the phase noise measured at the carrier frequency of 700 MHz. The measured result is -104.3 dBc/Hz at 100-kHz offset and -135.6 dBc/Hz at 1-MHz offset respectively.The VCO phase noise is -98.3 dBc/Hz at 100-kHz and -129.6 dBc/Hz at 1-MHz offset respectively after adding 6 dB, while consuming current of 7.7 mA from a supply voltage of 1.8V. Fig. 9(c) shows phase noise performance across the VCO frequency range at 1 MHz offset, which confirms the VCO has a good noise performance in the entire frequency range. In contrast, Fig. 8 shows the simulation result of the free running VCO at the carrier frequency of 1.4 GHz, which is close to the test result at 1 MHz offset.

A figure-of-merit (FOM) is employed to evaluate the four performance parameters of the VCO: frequency, phase noise, power consumption and frequency tuning range[13], which can be expressed as:

$$FOM_T = 20\lg\frac{f_o}{\Delta f} - 10\lg\frac{P}{1mW} - PN + 20\lg(FTR/10) \quad (5)$$

$$FTR = [(f_{max} - f_{min})/f_c] \times 100\% \quad (6)$$

Where f_o is the oscillation frequency, f_{max}, f_{min} are the maximal, minimal operation frequency, respectively, f_c is the center oscillation frequency, Δf is the offset frequency, P is power dissipation valued in mW, and PN is the phase noise valued in dBc/Hz.
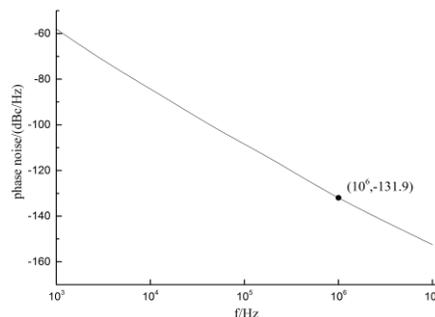

Fig.8. free running VCO output phase noise simulation result at 1.4 GHz

TABLE II
PERFORMANCECOMPARISONOF CMOS VCO

Ref	CMOS process (nm)	Power (mW)	Tuning range (GHz)	f_c (GHz)	Phase noise (dBc/Hz)	FoM$_T$ (dBc/Hz)
[7]	65	8	1.6~2.6	2.1	-124@1MHz	195.0
[8]	90	23	2.55~4.08	2.1	-126@1MHz	192.1
			4.9~5.75		-125@1MHz	181.9
[9]	180	18	1.35~2.05	1.7	-122@1MHz	186.3
			2.05~2.75	2.4	-119.5@1MHz	183.8
This work	180	14	1.02~1.77	1.4	-129.6@1MHz	195.7

Based on the measured results above, Table II summarizes the measured performance comparison of the VCO in this work with other recent state-of-the-art VCOs in published literatures. The wide frequency tuning range with the proposed scheme show better performance than the *LC*-VCO in [8] and the two *LC*-VCOs in [9] which have ordinary phase noise performance at higher oscillation frequency with higher power consumption. The *LC*-VCO reported in [7] has lower power consumption and ordinary phase noise performance at higher oscillation frequency, but utilizing a more expensive 65nm process.

5. Conclusion

In this letter, a wide-tuning-range low-phase-noise VCO is reported. An optimized switch structure and programmable *LC*-tanks are applied in the self-bias structure of VCO to optimize noise performance. The performance outcomes well validate the effectiveness of the topologies and methodologies used in the design. The fabricated VCO exhibits a tuning range of 53.8% from 1.02 GHz to 1.77 GHz, a phase noise of -129.6 dBc/Hz at 1 MHz offset from the carrier frequency of 1.4 GHz. The measured results show a wide tuning range, good noise performance of the presented *LC*-VCO.

6. Acknowledgment

7. References

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Fig. 9. (a) f-V tuning characteristic refers to the 7-bit binary-weighted digital codes, D<6:0>,(b) PLL output phase noise measured at 700MHz, (c)phase noise performance across VCO frequency tuning range at 1-MHz offset

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