A 3.4 GB/s Full-Swing 2^7-1PRBS generator Integrated with Fast-Locking PLL using Transmission gate Charge-Pump in 0.18- µm CMOS for HDMI applications

Ramanjaneyulu Ningampalli[1], Satyanarayana Donti[2] and SatyaPrasad Kodati[3]

***Abstract*—**This paper presents a 3.4 GB/s Full-Swing 2^7-1 Pseudo Random Binary Sequence (PRBS) generator with 3.4 GHz PLL in 0.18- µm CMOS. The proposed PRBS generator achieves 3.4 GB/s by using current mode XOR gate and current mode D flip-flops. The data jitter of the 3.4 GB/s PRBS output is 2.755ps with full-swing output voltage of 1.8 V. The High-Definition Multimedia Interface (HDMI) system includes a PRBS Generator driven by a Phased Locked Loop (PLL) which provides the source with test data. The proposed PLL can be locked from 2.539 GHz to 5.0793 GHz with a lock range of 2.54 GHz with 48.4% of duty cycle. The peak-peak jitter is 8.786 ps with an RMS jitter of 1.18 ps and pull-in time 180ns (fast lock-in time). The PLL consumes 18.8 mW power from a 1.8V power supply. The PRBS and PLL Blocks are simulated with 1.8V, 0.18- µm CMOS Technology using Cadence-Virtuoso tool.

***Keywords*—**HDMI, PRBS, Phase Frequency Detector, charge pump, delay Cell, Voltage Controlled Oscillator, PLL.

I. INTRODUCTION

Pseudo Random Binary Sequence (PRBS) generators are needed as test signals for digital electronic circuits and systems in the field of digital data communications. The High-Definition Multimedia Interface (HDMI) is used for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. HDMI is a digital replacement for existing analog video standards. At its heart, HDMI is a high-speed, serial, digital signaling system that is designed to transport extremely large amounts of digital data over a long cable length with very high accuracy and reliability **[1].** In order to achieve such high accuracy and reliability, HDMI uses Transition minimized Differential Signaling (TMDS**) [2]** to move information from one place to another. In this scheme, the data is encoded so as to reduce the number of 0-1 transition which in turn reduces the inter-symbol interference **[3].** The encoded data is then transmitted serially over the cable. The physical layer for TMDS is current mode logic, DC Coupled and terminated to 3.3V.The use of Current Mode Logic (CML) ensures superior performance in noisy environments and in the presence of lossy transmission lines. The required specifications as per the HDMI Specification version 1.4 are given in the Table I.

Table I. HDMI 1.4 specifications

Parameter	**value**
Supply voltage	3.3V
Data rate	3.4GB/s
Tx signal swing(single ended)	400mV to 600mV
Single ended high level output voltage V_H	3.1 V to 3.3 V
Single ended low level output voltage V_L	2.6 V to 2.9V
Rise time/Fall time	>75ps

To avoid using expensive high-speed test equipment, on-chip PRBS generators have been developed to provide a cost effective way to HDMI transmitter. The jitter performance of the HDMI transmitter can be measured through the received eye diagrams produced by the PRBS.

The phase-locked loop (PLL) circuit used in HDMI applications must have a fast pull-in time and low jitter. Phase locked-loops (PLLs) are widely used to generate well-timed on-chip clocks in high-performance digital systems. For clock generation, since off-chip reference frequencies are limited by the maximum frequency of a crystal frequency reference; a PLL receives the reference clock and multiplies the frequency to the multi-gigahertz operating frequency. The high-frequency clock is then driven to all parts of the chip. Timing recovery pertains to the data communication between chips **[4].**

The rest of this paper is organized as follows .Section II presents the proposed block diagram of PRBS generator and its simulation results. Section III presents the individual working blocks in proposed PLL. Simulation results of a PLL are given in Section IV and the conclusion is given in section V.

II. PRBS GENERATOR

A. Requirement for PRBS Generator

In order to test the designed transmitter circuit, a differential data signals at the rate of 3.4 Gb/s is required. In order to generate this test input signal, we require a Pseudo Random Binary Sequence (PRBS). The PRBS should produce a Pseudo-random differential binary sequence at the required operating frequency of 3.4 GHz.

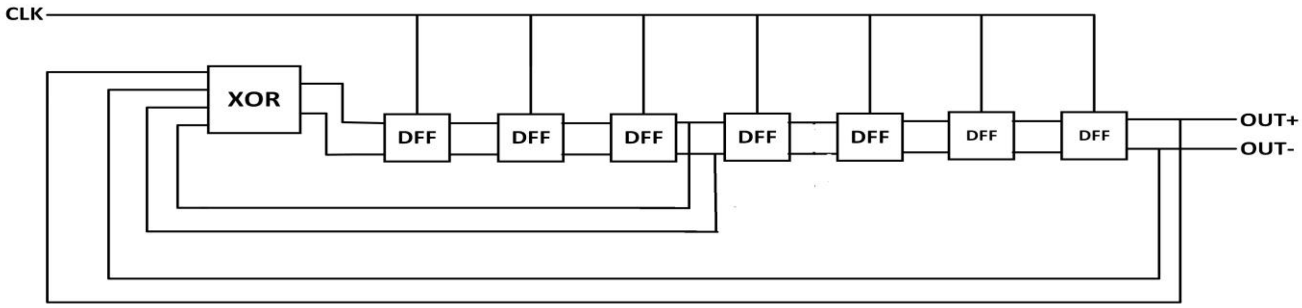

Fig1. LFSR for Polynomial $P(x) = X^7+X^3+1$

The PRBS Generator is realized by means of a Linear Feedback Shift Register (LFSR). Since we require a differential output bit stream, the LFSR should also be differential in nature. Thus, current-mode XOR gate and current-mode D Flip-flops were used for building the PRBS Generator. The block diagram of the 7-bit differential PRBS Generator is shown in fig 1. The seven D-Flip flops are connected serially to form a shift register. The output of the seventh flop-flop and third flip-flop are feedback as inputs to the current-mode XOR-gate. The output of the XOR gate is fed as input to the first flip-flop. A clock signal at 3.4GHz is given to all the flip-flops. The PRBS then generates a random bit-stream at the same frequency**.** A conventional current-mode XOR gate is implemented as shown in fig 2.

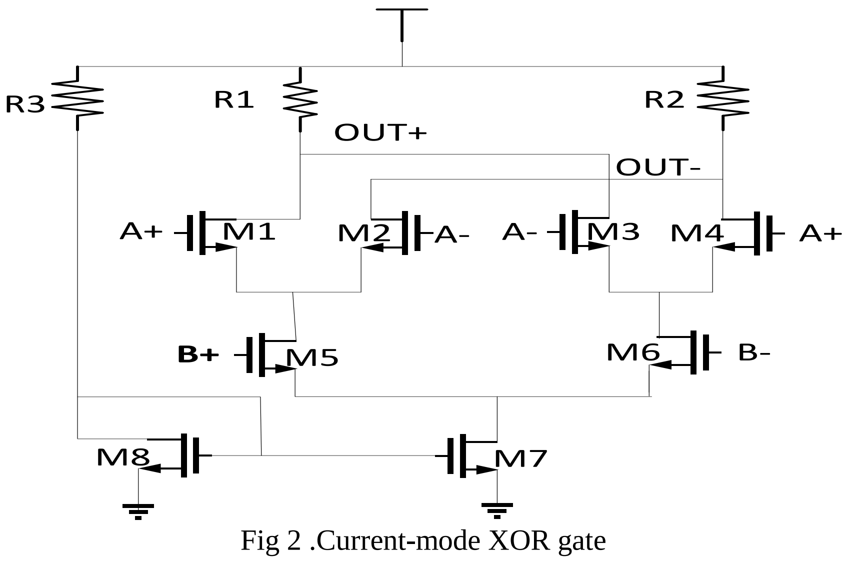

Fig 2 .Current-mode XOR gate

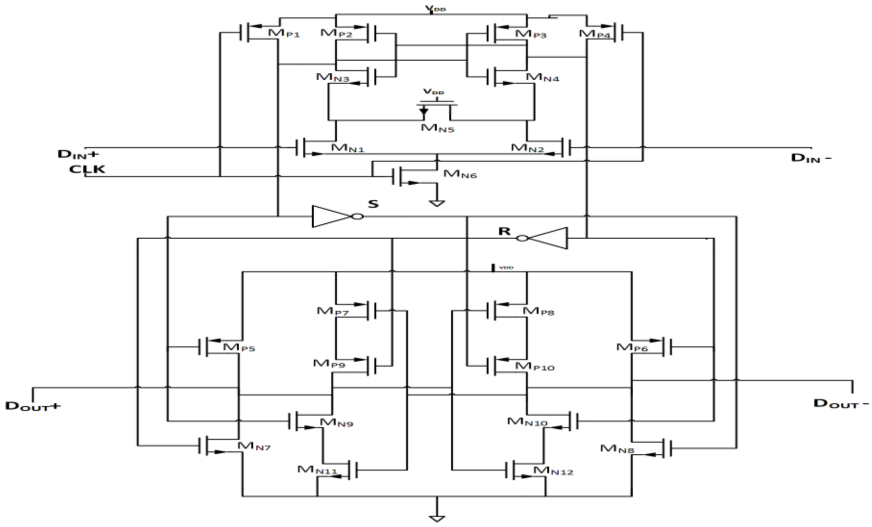

Fig3. Sense amplifier based flip-flop

The sense amplifier based flip-flop uses a new output stage latch topology shown in fig 3 that significantly reduces delay and improves driving capability **[5].** All flip flops were optimized for minimum delay and reduced output transistor sizes. A clock signal at 3.4GHz generated from PLL is driving all the flip-flops. The PRBS then generates a random bit-stream of length127cycles at the same frequency.

B. Simulation Results

The single ended output waveform of the PRBS Generator is shown in fig 4. The binary-sequence repeats itself after 127 cycles. The V_{high} and V_{low} for the single-ended outputs are 1.8V and 0V respectively. The eye diagram of the PRBS Generator is shown in fig 5 which operates at 3.4GB/s the measured jitter of PRBS generator is 2.755ps.Table II shows the performance summary of the designed PRBS Generator.

Table II. Performance summary of the designed PRBS Generator.

Parameter	**Value**
Frequency	3.4 GB/s
Output Voltage Swing	1.8V
Jitter (ps)	2.755
Length of random sequence	127
Max. Power(mW)	33

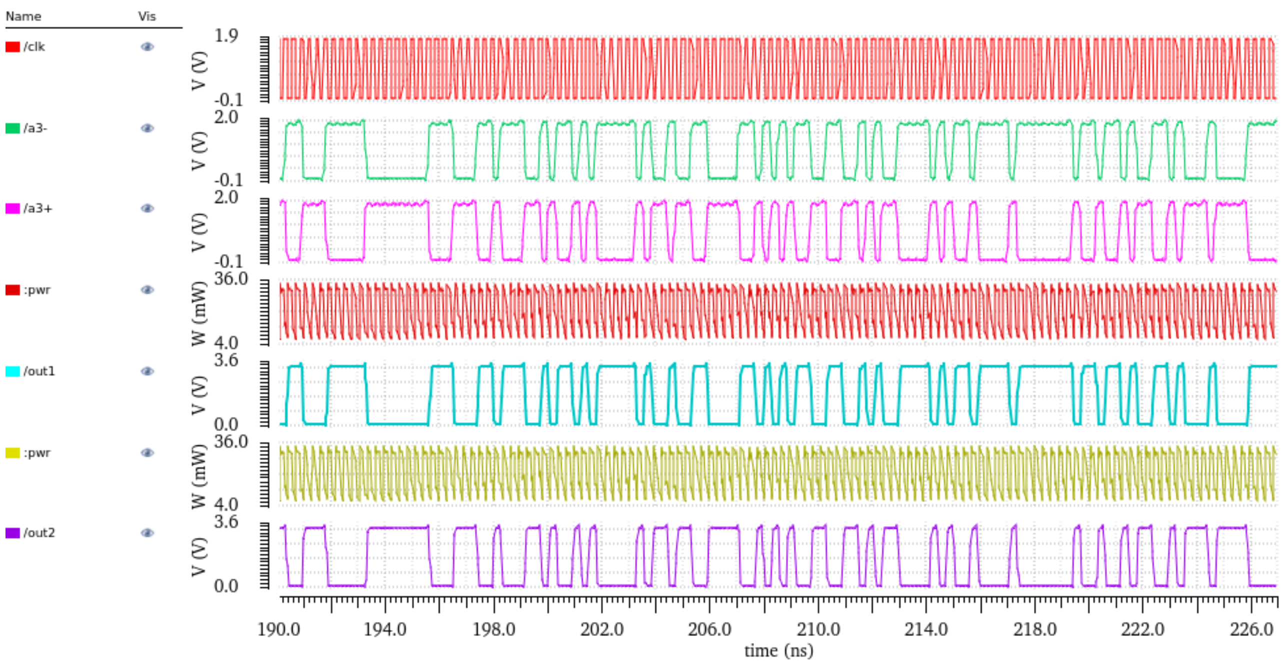

Fig4. Double ended output waveforms of the PRBS Generator.

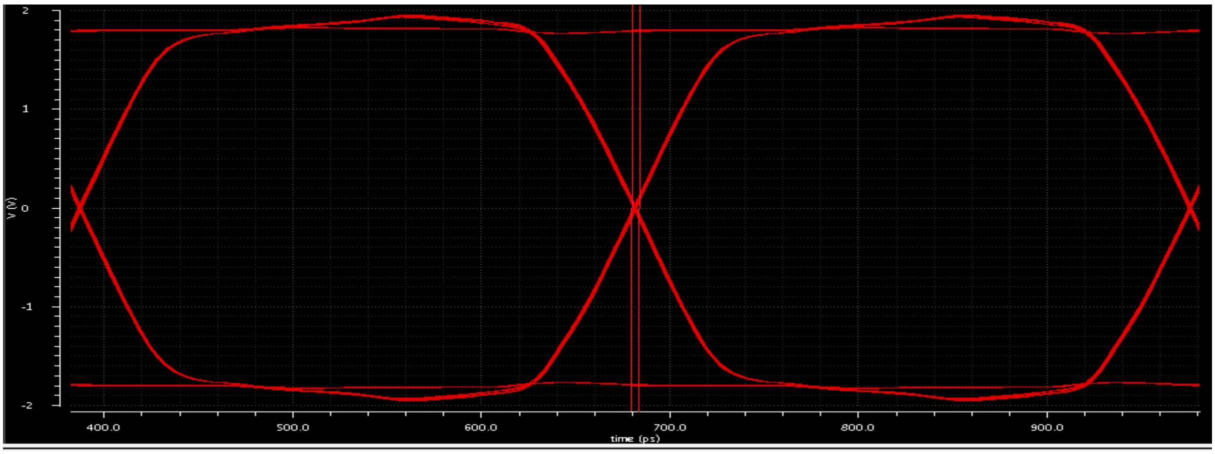

Fig5.Eye diagram of the 3.4 Gb/s PRBS Generator (2.755ps jitter)

III. PROPOSED PLL BLOCK DIAGRAM

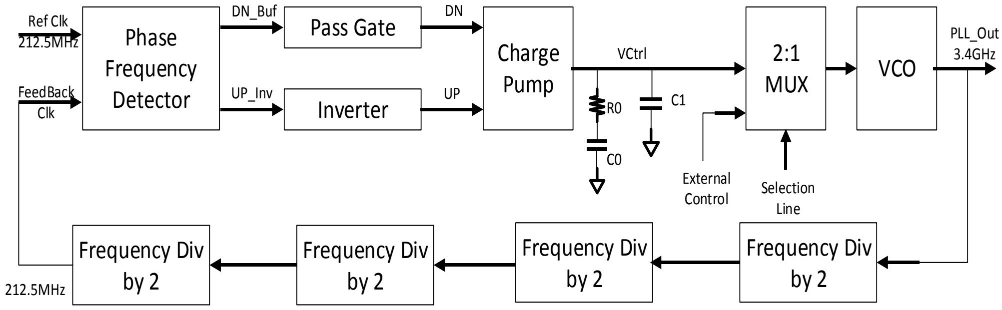

Fig6. Block diagram of the proposed PLL.

The proposed PLL is composed of mainly six blocks is shown in fig 6.

a. Phase Frequency Detector (PFD)
b. Charge Pump (CP)
c. Low Pass Filter (LPF)
d. 3.4 GHz Voltage Controlled Oscillator (VCO)
e. Divide by N Counter

The main advantage of the proposed PLL is by using a 2:1 Multiplexer (Mux) the same design may be used either VCO or complete PLL circuit. If selection line=0, then the circuit perform PLL operation otherwise VCO operation. The 2:1 mux is designed with the pass gate logic so that the design can pass the control voltage without any drop.

A. Phase Frequency Detector (PFD)

PFD produces an error output signal proportional to the phase difference between the phase of the reference clock (Φ_{in} (t)) and the generated clock (Φ_{Out} (t)). The relationship between the duty cycle of the error signal ($V_e(t)$) and the phase difference is linear. The ratio V/rad is defined as the gain of PFD (K_D).

$$V_e(t) = K_D\left[\Phi_{out}(t) - \Phi_{in}(t)\right] \qquad \textbf{(1)}$$

The PFD has 2 inputs namely reference clock and the feedback clock. Up (UP) and Down (DN) signals are its outputs as shown in fig 7. If there is a phase difference between the two input signals, it generates UP or DN synchronous signals to the charge pump with the duty cycle of the signals proportional to the phase difference between the two input signals **[6].**

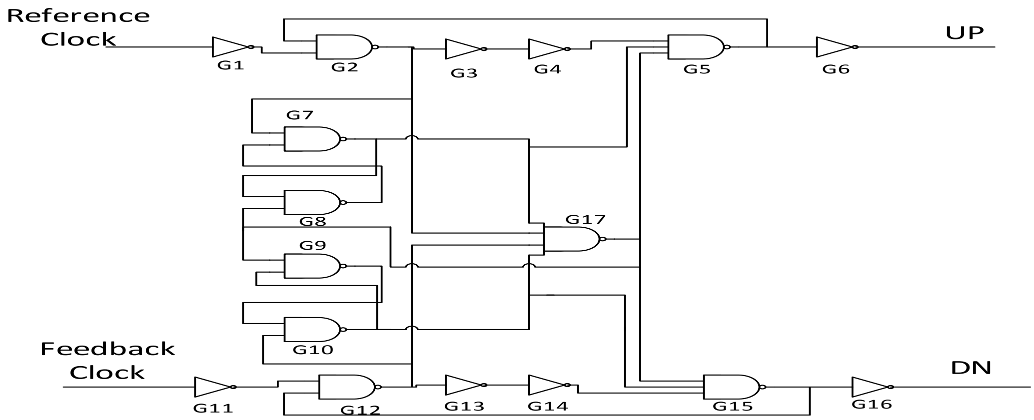

Fig7. Schematic of a PFD

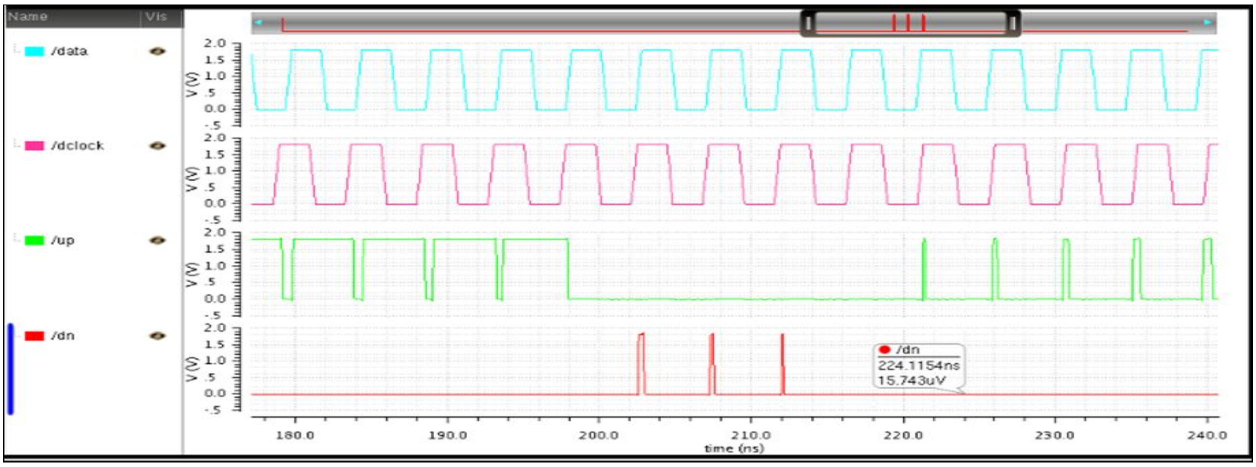

Fig8. Output waveform of a PFD

If the rising edge of the reference clock leads the feedback clock, the UP output of PFD goes high while the DN output remains low. This causes the increase in the frequency of feedback clock. When the feedback clock leads the reference clock, Up remains low and the Down signal goes high till the time equal to phase difference between reference clock and the clock generated. When the loop is in locked state i.e., both the frequency and phase of the reference clock and the clock generated are matched, the output Up and Down signal should remain low. The schematic of PFD is shown in fig 7. The PFD detects the phase difference and produces a pulse on UP and DN signals. The PFD has been found to work under different process corners. The output waveform of a PFD at typical corner, 1.8V and 27^0C is shown in fig 8. Table III compares the proposed PFD with recent works [7]-[9].The proposed PFD consumes low-power. This is lower than previously reported PFD circuits.

Table III : The proposed PFD performance comparison

Performance parameter	**[7]**	**[8]**	**[9]**	**This work**
CMOS tech(µm)	0.18	0.35	0.18	0.18
Power supply(V)	0.8	3.3	1.8	1.8
Max. freq. (GHz)	1	2	8	5.4
Dead-zone	Free	Free	Free	Free
Power consumption (mW)	NA	4.65	0.5	0.065
Structure	Close	Open	Open	Open

B. Charge Pump

A Charge pump sinks or sources current for a limited period of time depending on the UP and DN signals [6]. UP signal is inverted and passed to Charge pump because the pull up network is controlled by the PMOS transistors. DN signal controls the pull down network. To compensate the delay caused by the inverter for UP signal, the DN signal is passed through a pass gate. The control voltage (VCtrl) is the output of charge pump. It will increase or decrease the VCtrl depending on the UP or DN signals respectively. The schematic of a CP is shown in fig 9.

When the Up signal is low (pull up network is on) and the Down signal is also low the output capacitance charges through M1 and M3 and the VCtrl rises. Similarly when the Down signal is high (M2 and M4 on) and the Up signal is high (M1 and M3 off) yields a drop in VCtrl since the output capacitance discharges.

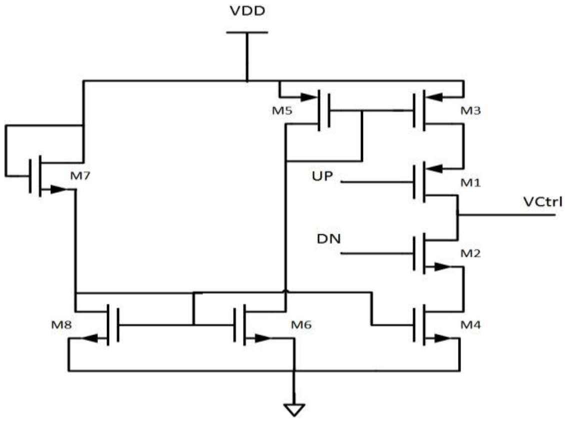

Fig9. Schematic of a CP

The Charge pump should be designed in such a way that same current flows through M1 - M4 when both the UP signal and the DN signal is low which should keep the VCtrl constant. Otherwise there will be a charge sharing between the parasitic capacitance on the drains of pull UP and DN networks and the capacitance used in the loop filter causes a static phase error or jitter. When only the M1 and M3 are on the amount of current flowing from Vdd to output capacitance should also be same as the amount of current that flows from output capacitance to ground when only M2 and M4 are on.M5 to M8 transistors act as current source. So the devices should be properly sized in such a way that it obeys the above conditions. Also the jitter should be low for the above sizing. The current mirrors are sized in such a way that they provide sufficient current for the charge pump to produce the required control voltage.

B.1 proposed Transmission gate Charge Pump with Extra Current Paths

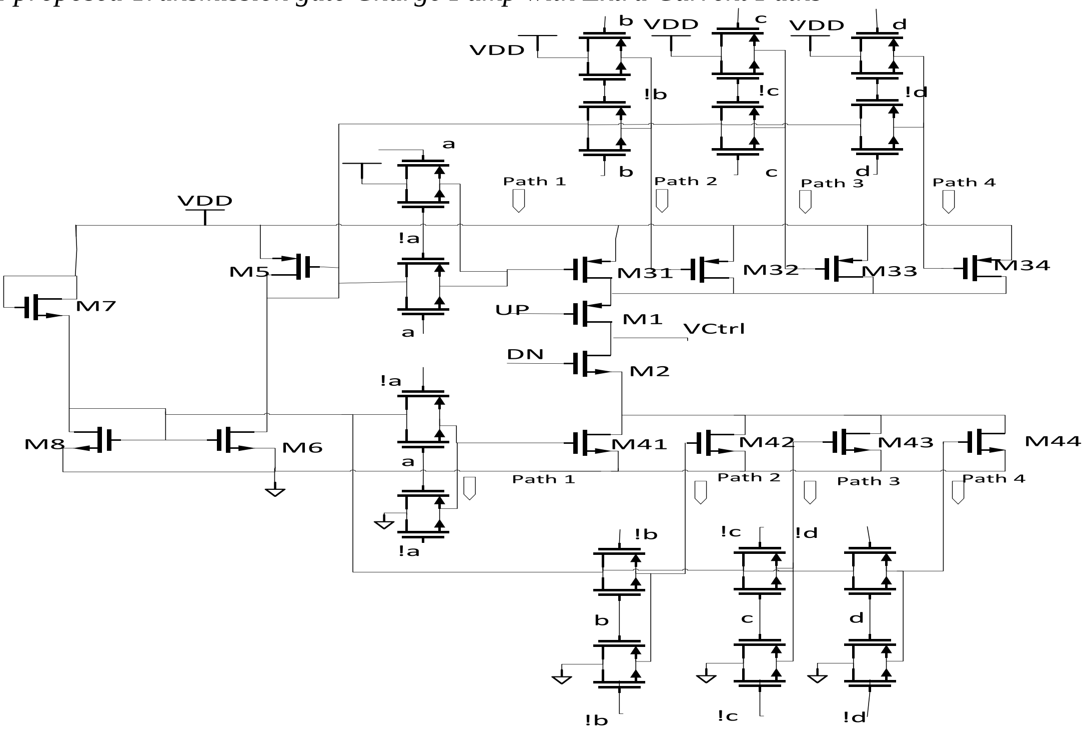

Fig10. Schematic of a proposed Transmission gate charge pump

If there is a need to increase the current or reduce the current, the Transmission gate Charge pump is provided with more than one path which is controlled by transmission gate switches is shown in Fig 10. The ON/OFF of these switches determines whether to increase or decrease the current. The sizing of the transistors in each path is done so that the amount of the current doubled from one path to other, so that we can make combinations of different currents to produces stable control voltage and can lock the system quickly. Currents measured in 4 paths are path 1=65μA, path 2=130μA, path 3=260μA and path 4=520μA.

Table IV: Performance comparison of the proposed charge pump

Performance parameter	**[10]**	**[11]**	**[12]**	**[9]**	**This work**
CMOS Process(μm)	0.18	0.18	0.18	0.18	0.18
Power supply (V)	1.8	1.8	1.8	1.8	1.8
Voltage swing	0.4-1.2 V	0.4-1.25V	0.3-1.58V	0.25-1.6V	10nv-1.8V
Swing/Vdd (%)	44	47	71	75	99.9
Constant current magnitude	no	yes	yes	yes	yes

Table IV compares the proposed charge pump with recent works [9-[12]. As can be seen, all parameters of the proposed charge pump circuit are improved compared with the other charge pump circuits.

C. Loop Filter

The output of the PFD consists of a dc component and a high frequency component. But the control voltage of the oscillator must remain quiet in steady state. So by using a passive second order low pass filter (LPF) the high frequency components can be removed and present only the dc level for control voltage (VCtrl). The output of the loop filter is VCtrl .The second order LPF has the smallest resistor thermal noise and largest capacitor next to the VCO to minimize the impact of VCO input capacitance.The filter also has maximum resistence to variations in VCO gain and charge pump gain. To improve the phase margin and thus stability, minimize the large jump experienced by the control voltage, a second order loop filter is used as shown in Fig 11.

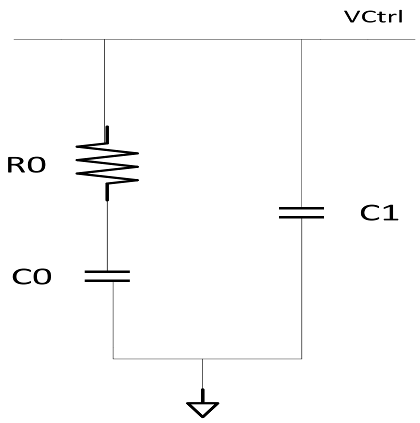

Fig11. Schematic of a second order loop filter

The values of R0, C0 and C1 are R0= 2.5KΩ, C0 = 5pf, C1 =2.5pf.

D. Voltage Controlled Oscillator (VCO)

The VCO is an important component in PLL. Conventional VCOs offering many significant advantages have been developed [13]-[21].Since the output must have low jitter, high linearity and high supply noise rejection. In this application the VCO is designed using differential delay cells in a ring oscillator manner. The VCO has 3 delay cells. The differential delay stage advantage is that, ideally, noise on the supply appears as common-mode on both outputs, and is rejected by next stage in a chain.

Delay Cell

The schematic of a delay cell is shown in fig 12**.**In this fig M1 & M2 NMOS input transistors designed for required gain and bandwidth .M5 & M6 NMOS cross coupled transistors to provide positive feedback. M3 & M4 PMOS transistors serving as current source loads and provide designed current for operating frequency. The current is used by the delay cell to produce output frequencies. First based on the control voltage, the VB will get corresponding voltage to ON the PMOS transistors in Delay cells. Based on the VB, the current driving into the circuit varies and the frequency of the VCO changes. Hence the frequency generation is completely dependent on the current driving through the PMOS network. The operating frequency is nominally controlled by adjusting the PMOS transistors' current. Cross-coupled pairs are adopted to guarantee oscillation with differential outputs. The design is similar to the Lee–Kim delay cell [22]. Unlike the Lee–Kim cell, NMOS transistors are used in the cross-coupled pairs instead of PMOS transistors for a higher operating frequency [23]. The existence of the zero supply sensitivity and the magnitude of both the positive and negative supply sensitivity depend on the design parameters such as the transistors' width, length, and the P/N size ratio of the delay-cell transistors [24]. The differential delay stage strength is that, ideally, noise on the supply appears as common-mode on both outputs, and rejected by next stage in a chain.

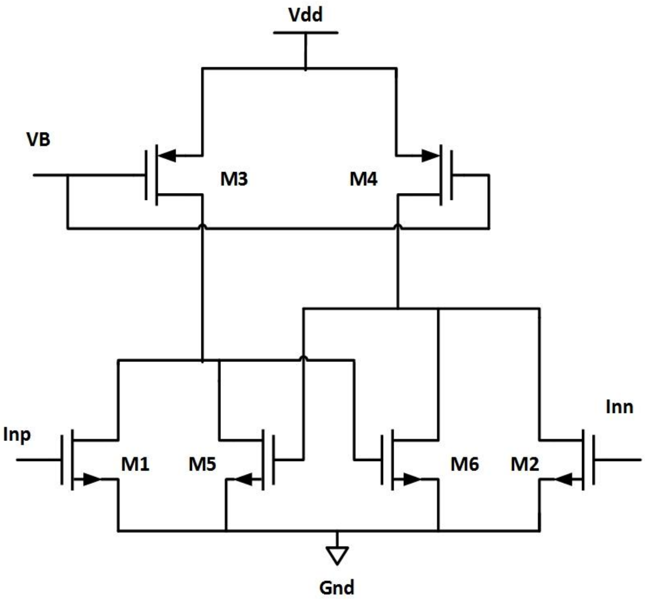

Fig12. Schematic of Differential Delay Cell

The complete schematic of the 3 stage VCO is shown in fig 13.In this fig M1, M2 and R form a Voltage to Current (V-I) converter, to convert Vctrl to the current. This current acts as a bias current for all 3 delay elements in the VCO circuit. The transistor goes from saturation region of operation to triode region of operation if the control voltage crosses 1.15V. So the output frequency of the VCO varies in a nonlinear fashion. In the 3.4GHz range the VCO is linear. The linearity is achieved over a wide-range of frequency from 1.76GHz to 3.4GHz.

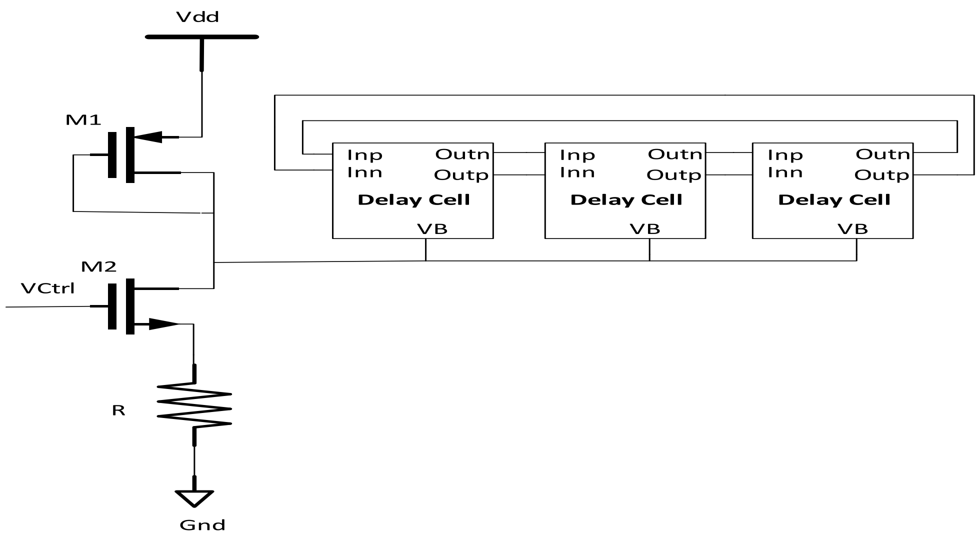

Fig13. Schematic of Differential Ring Oscillator

.The output wave form of a VCO at typical corner is shown in fig 14.The output frequency of VCO is 4GHz. The test case is done by giving 1.2V control voltage and transient analysis is performed. The phase noise of the Proposed VCO is -140 dBc/Hz at 3.5 GHz is shown in fig 15.Table V shows the performance summary of the proposed VCO.

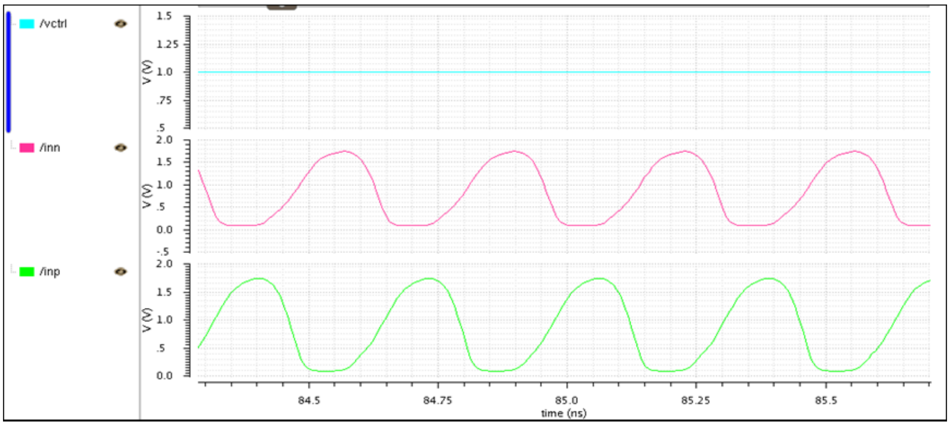

Fig14. Output waveform of a VCO

Table V: Performance summary of proposed VCO

VCO parameters/Process corners	TT	SS	FF	FNSP	SNFP
Control voltage (Vctrl) (V)	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**
Frequency (GHz)	3.42	2.8	4	3.52	3.28
Linearity (GHz)	1.76 to 3.4	1.5 to 3.8	2.5 to 5.2	2.2 to 4.58	1.9 to 4.8
Tuning range(%)	48	60.52	51.9	51.9	60.4
output Noise (dBc/Hz) @3.4GHz	-133	-135	-132	-118	-108
Phase Noise (dBc/Hz) @3.4GHz	-138	-140	-136	-124	-116
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8

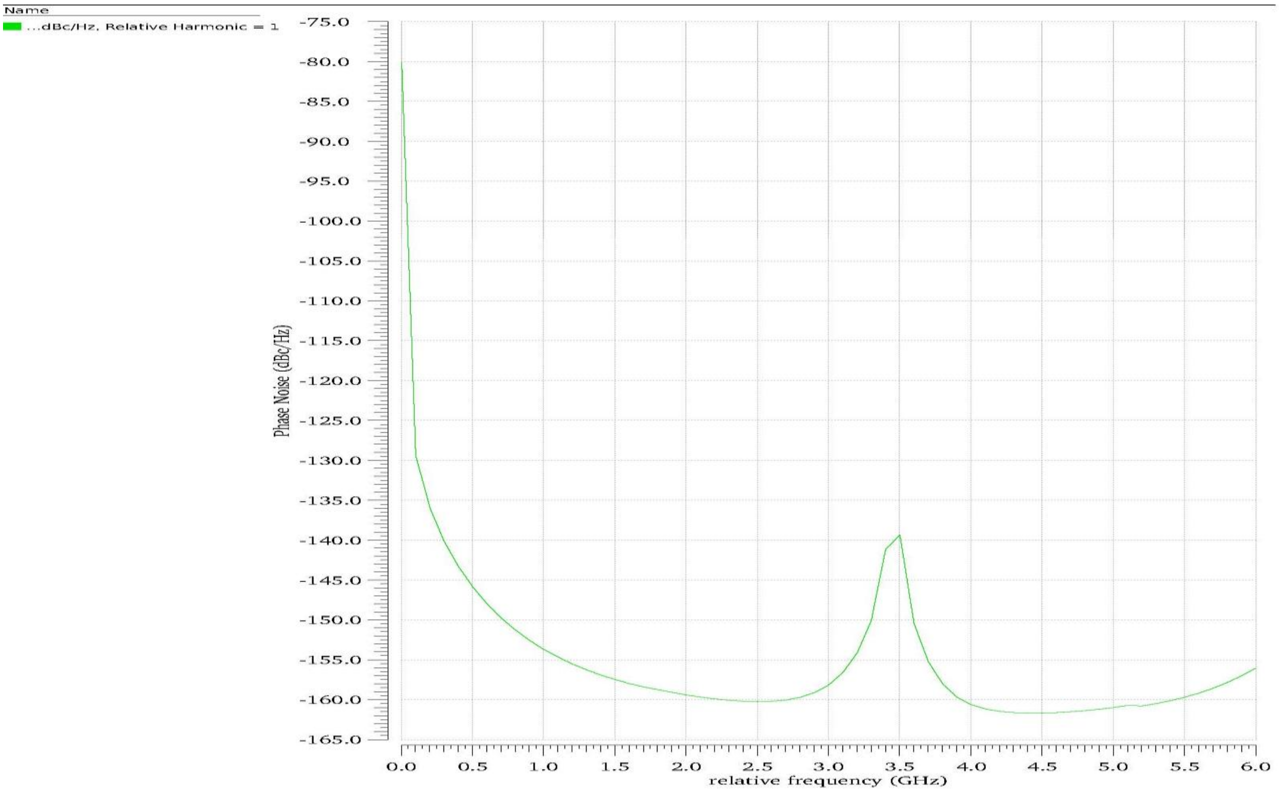

Fig15 .Simulated Phase noise at 3.5GHzfor different relative frequencies

The VCO has been found to work under different process corners. Fig 16 shows the VCO frequency versus different process corners when control voltage is VDD/2 i.e 0.9V.Fig 17 shows the VCO tuning range versus process corners. It is found that under SS (Slow-slow) corner the VCO achieved highest tuning range.

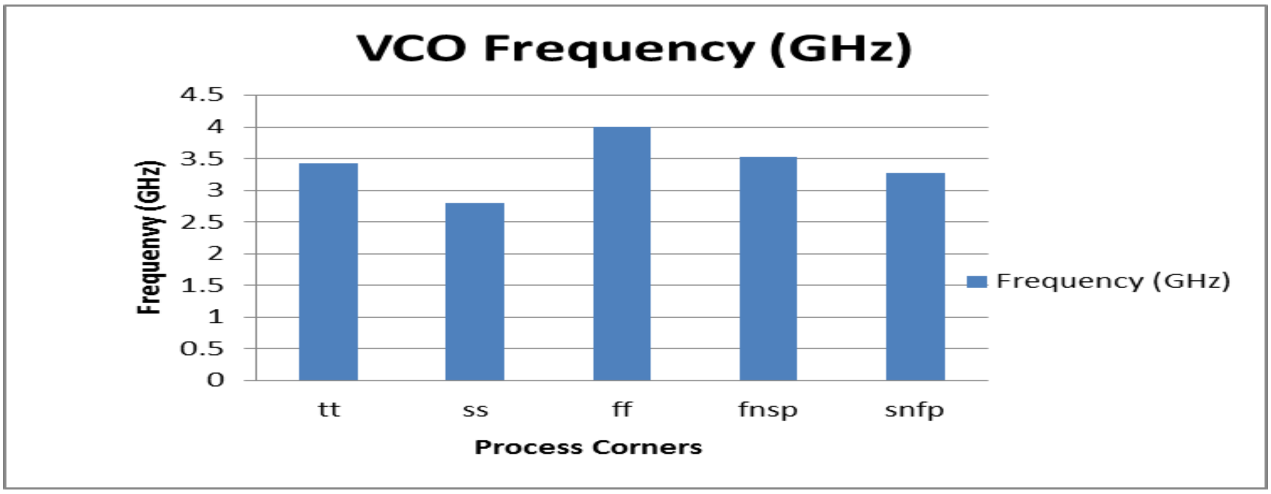

Fig16. VCO frequency versus Process corners (Control voltage=0.9V)

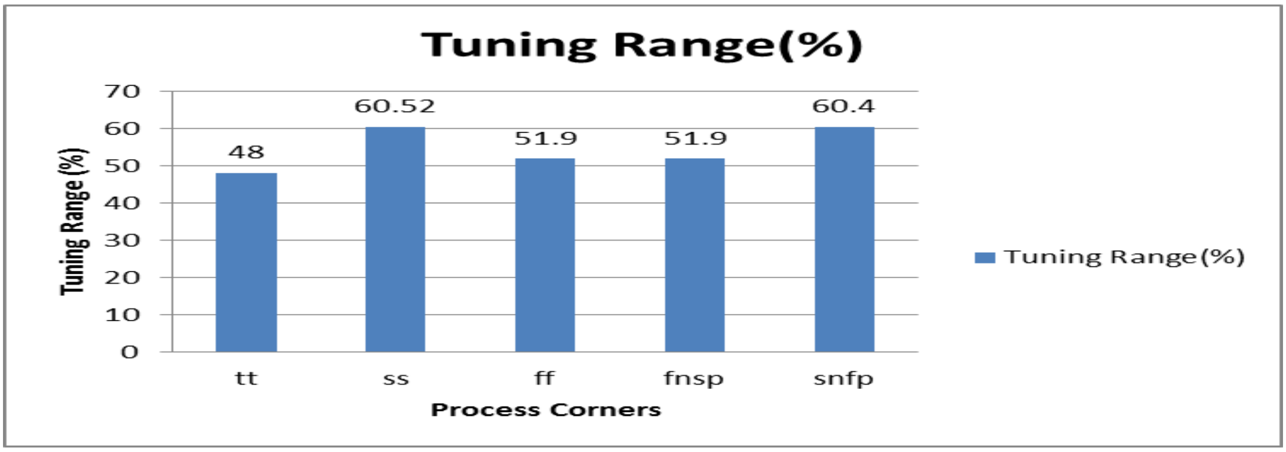

Fig17. VCO Tuning range versus Process corners (Control voltage=0.9V)

E. Frequency Divider

Frequency divider circuit plays an important role in PLL design **[25]-[26].**The T Flip-flop is implemented using D Flipflop. The D-FF is designed using the TSPC **[27]** so that the 0-0 and 1-1 clock overlaps will not occur.

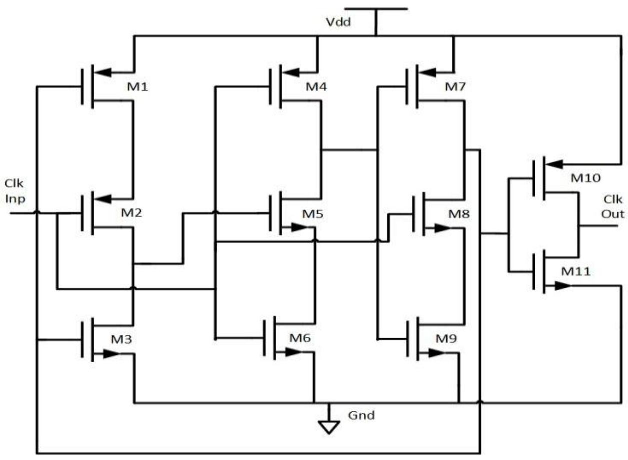

Fig18. Schematic of a divide by 2 cell

The schematic of a divide by 2 cell is shown in fig18. To implement divide by 16 frequency divider four T Flip-flops are cascaded together. To avoid race conditions in TSPC, M5 and M6 W/L values should be made larger than M8 and M9. The frequency divider has been found to work under different process corners.The output waveform of a frequency divider at typical corner, 1.8V and 27^0C is shown in fig19.

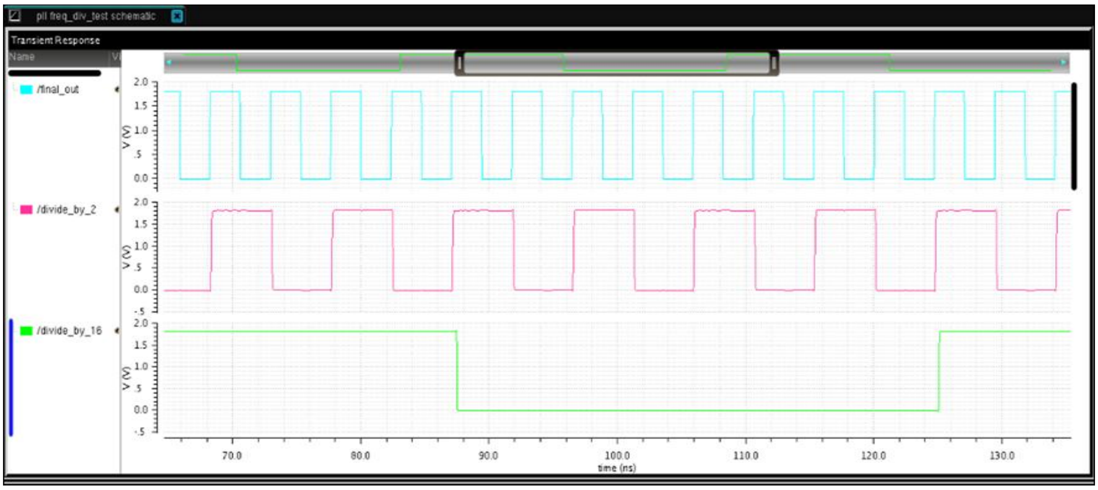

Fig19. Output waveform of a frequency divider

IV. PLL ANALYSIS AND RESULTS

A. PLL Working

PLL ensures that the clock generated tracks the reference clock and then it is said to be locked. If the loop is locked the clock generated and the reference clock has same frequencies but a finite phase difference exists and the PFD generates pulses whose width is equal to constant phase difference. These pulses are filtered to produce the dc voltage (average value) that enables the VCO to operate at a frequency equal to the reference frequency. The constant phase difference is the static phase error.

If the reference frequency is greater than the frequency of clock generated, reference clock accumulates the phase faster and the phase error grows high. So the PFD generates the increasingly wider pulses raising the dc level at the output of the LPF and hence the frequency of VCO increases. The difference in the frequency between the reference clock and the clock generated diminishes. Eventually the width of the PFD output pulses settles to a value. The loop locks only after two conditions are satisfied. One is the frequency of the reference clock and the clock generated are same and the other is the phase difference between them should settle to proper value.

If the output phase error of PLL varies with time, we say the loop is unlocked. Also if the VCO start up frequency is far from the reference frequency, the loop may never lock. The output frequency of PLL can be divided and then feedback. Since we have used the divide by 16 frequency divider at the feedback, we can generate the output of VCO with 16 times the frequency of reference clock. Thus the output of divider stage will be again at the same frequency as the reference clock. So we generate the output frequency which is a multiple of input frequency by a factor of 16. Here the input reference clock period is 4.7058825n (212.5MHz) and a divide by 16 stage is used. So the output frequency of VCO will be 294.117ps (3.4GHz.The block diagram of a proposed PLL is shown in fig 6.

B. Simulation results of PLL

The simulation of each block is done in Cadence Virtuoso. The schematic level design is done using tool Spectre in schematic editor. The layout is done and verified using the tool Assura. The simulation is done in 1.8V, 0.18 µm CMOS technology which takes into account the device parasitics.The results of each block is tested for PV conditions.The PLL has been found to work under different process corners and voltage (PV) conditions; the output waveform of PLL at typical corner is shown in fig20. PLL can lock from 2.539 GHz to 5.0793 GHZ by varying the reference frequency. So the locking range of PLL is 2.54 GHz

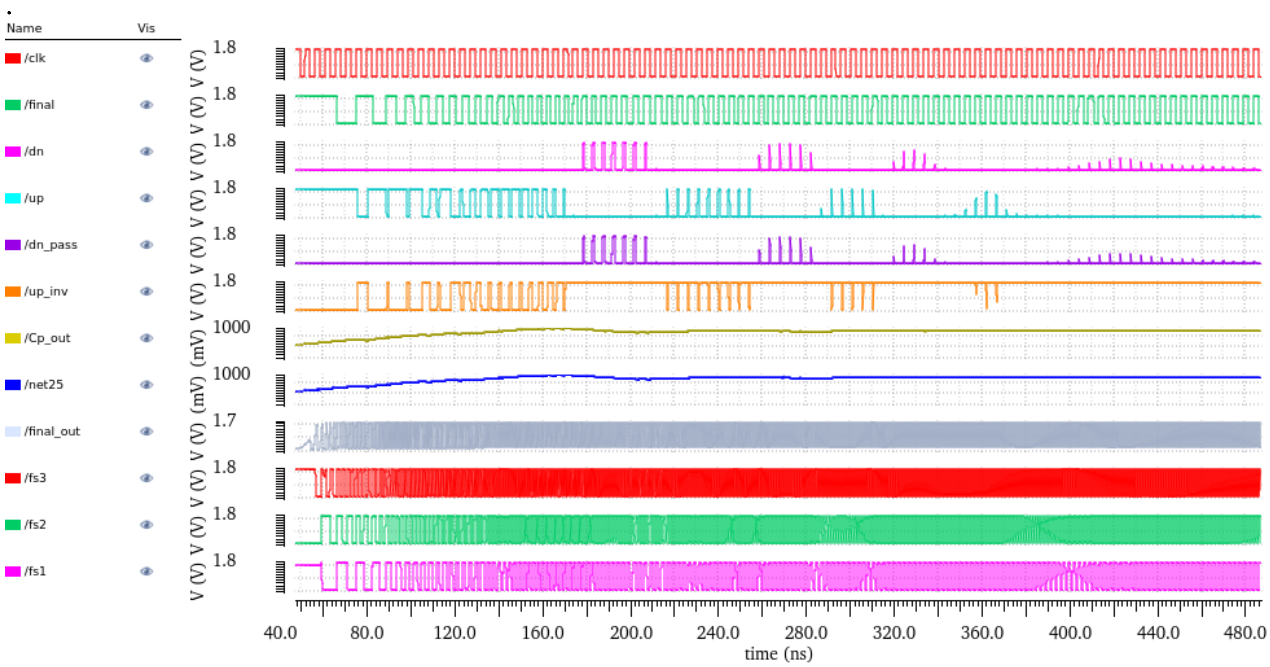

Fig20. PLL at Typical corner (TT) at 27^0C, 1.8V

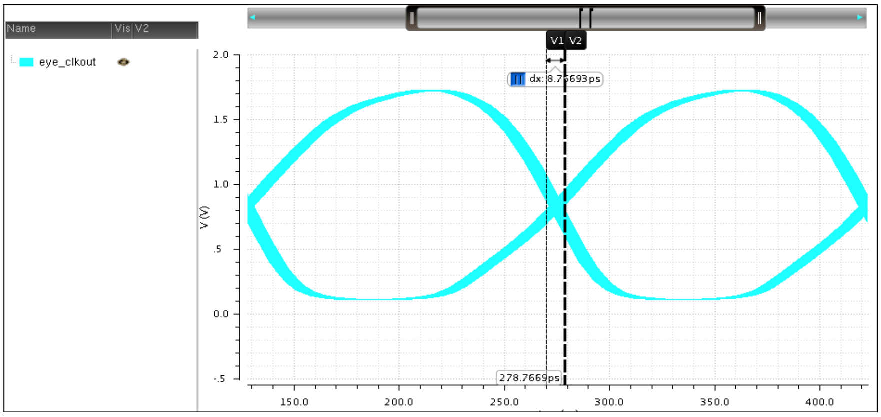

Fig21. Eye Diagram at 3.4 GHz clock (jitter8.786 ps)

Jitter is one of the importance performance parameter. Jitter is related to the power of noise of the PLL. The peak to peak jitter is measured for the final 3.4 GHz clock is 8.786 ps as shown in Fig 21. The jitter we observed by the overlapping of 2500 cycles, the calculated RMS jitter is 1.18 ps. The proposed PLL achieves lowest RMS jitter compare to recent works [28] to [34]. The complete PLL block consumes 18.8 mW of power from 1.8V supply. PLL-jitter results with power supply variations under typical corner are given in table VI.

Table VI: PLL-Jitter with power supply variations

Voltage	Jitter(P-P) in Ps	Jitter(RMS) in Ps
1.7	7.060	0.948
1.8	8.786	1.18
1.9	11.075	1.488

The commonly used **figure of merit** (FOM) is described by the following expression.

$$FOM = POWER / FREQUENCY \quad \textbf{(2)}$$

The proposed design has achieved the lowest FOM of 4.638pJ/Hz.

PLL **pull-in time** is one of the important parameter. Pull-in time is related to the fast-locking of the PLL system. The proposed PLL has been found that it achieves lowest pull-in time i.e fast-locking system. The simulated pull-in time is shown in fig 23.Fig 22 shows the PLL **output noise** with different relative frequencies. The output noise is -196 V/sqrt(Hz) (dB) at 3.4 GHz.

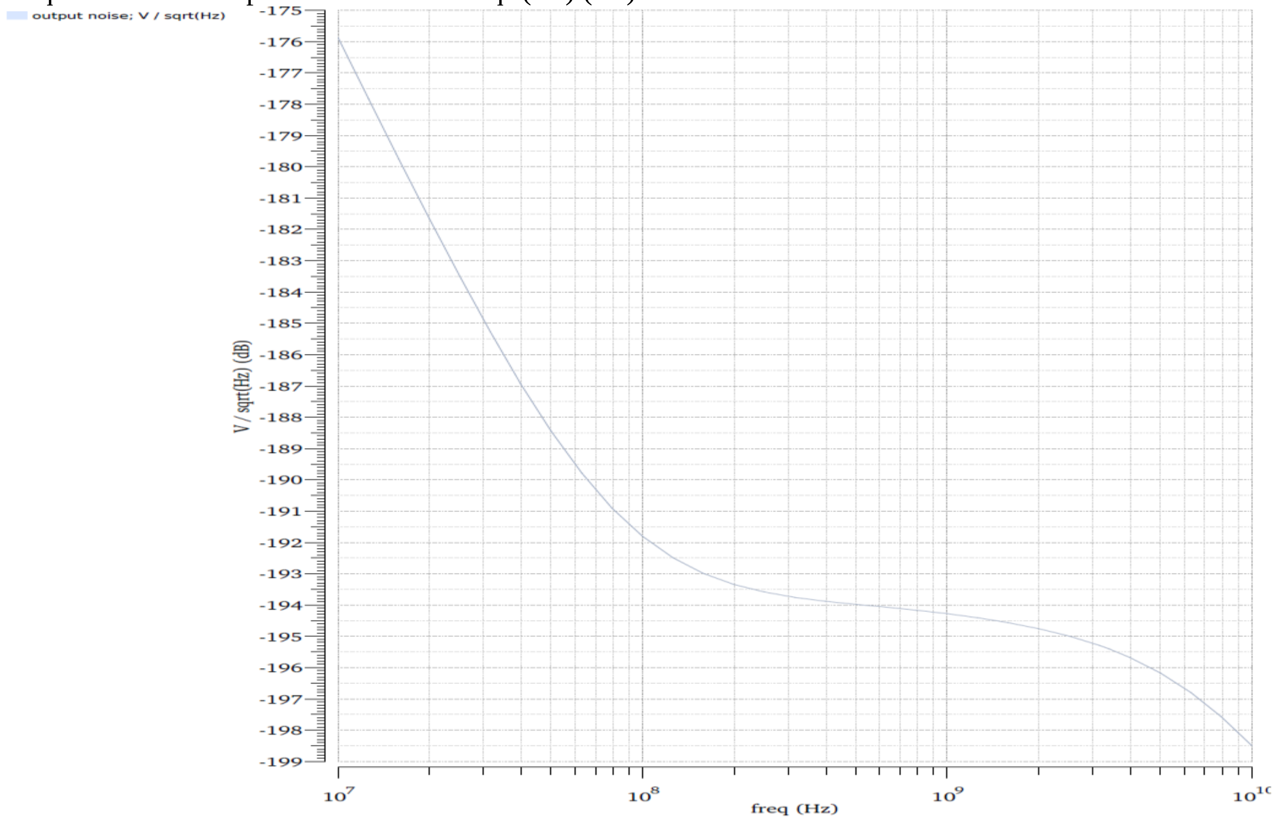

Fig22. Simulated output noise for different relative frequencies

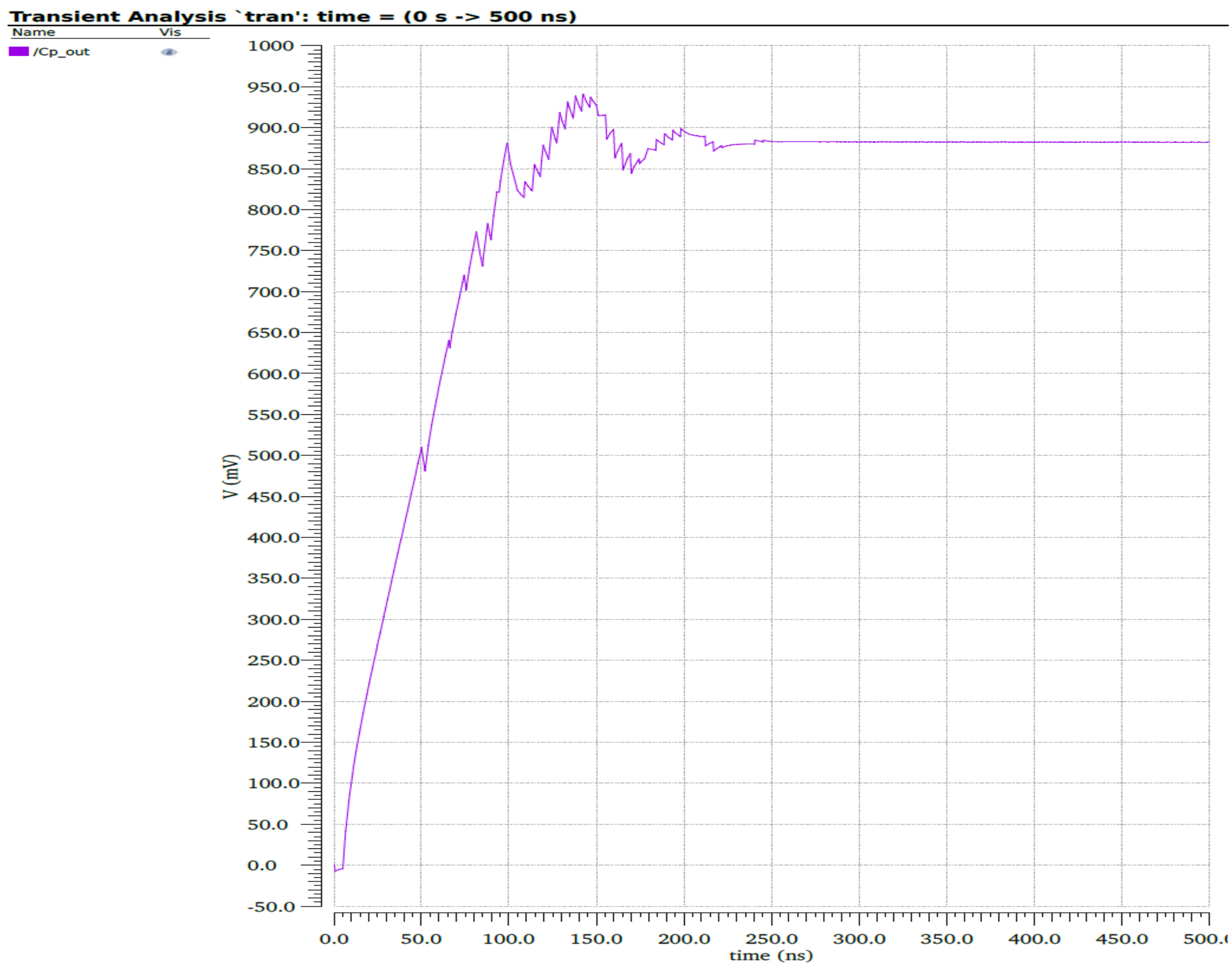

Fig23. Simulated PLL pull-in time (240ns, Path=1, fnsp)

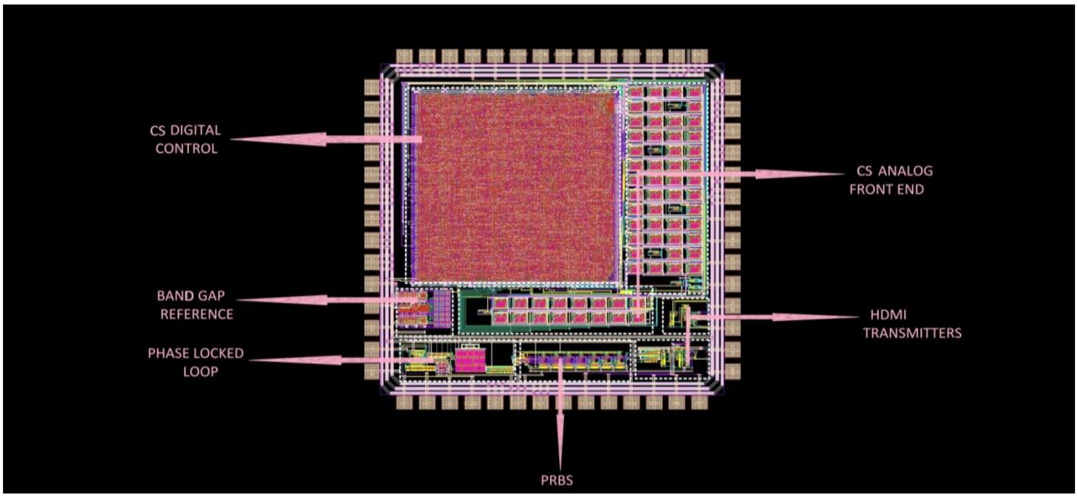

Fig24. Complete Test Chip

The complete test chip is shown in the fig24 with size 1000µm * 1000µm. The bottom left portion of the test chip shows the PLL. The other blocks that the test chip contain are PRBS, HDMI Transmitters, Band gap Reference and the compressed sensor. The PLL occupies **10 pins** in the test chip namely for reference clock, selection lines (4) to control the current through charge pump, selection line for feeding the control voltage directly to VCO, control voltage, Vdd, gnd and 3.4 GHz clock out. Table VII shows the performance comparison of PLLs with prior works [28]-[34] and [9].The proposed PLL achieved lowest RMS jitter and fast locking time.

TABLE VII: PLL PERFORMANCE COMPARISION

Performance Parameter	[28]	[29]	[30]	[31]	[32]	[33]	[34]	[9]	This work
CMOS Process(µm)	0.18	0.090	0.13	0.065	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	0.6	0.5	0.5	1.2	1.8	1.8	1.8	1.8	1.8
Locking range (GHz)	2.4-2.64	0.4-2.24	0.4-0.433	0.06-1.48	1.28-1.6	0.64-0.8	0.5-1.5	2.5-7.3	1.5-3.8
RMS jitter (Ps)	NA	2.22	5.5	8.03	8.789	NA	NA	3.21	1.18
P-t-P jitter (Ps)	NA	17.89	49.1	55.6	45	30	24	0.35	8.786
Locking time	NA	NA	NA	NA	NA	6 s	NA	0.35µs	0.170µs
Power (mW)	14.4	2.08@2.4GHz	0.44	4.3	NA	5.14	0.32	13.4	18.4
Results	Measured	Measured	Measured	Measured	Measured	Simulated	Simulated	Simulated	Simulated

Table VIII shows the Proposed PLL performance with normal charge pump. Table IX to XII shows the proposed PLL performance with proposed Charge pump with transmission gates using path 1 to path 4 respectively. Fig 25 to 27 shows the proposed PLL duty cycle, Pull-in time and Max.power consumption with different process corners and variation of different current paths in charge pump circuits.

Table VIII: PLL performance (normal CP)

PLL parameters/Process corners (Normal CP)	TT	SS	FF	FNSP	SNFP
Control voltage (V)	0.9	1	0.82	0.88	0.92
Max. Power (mW)	19	18.8	22	19.4	18.5
Pull-in time (ns)	320	295	not locked	380	650
Duty Cycle (%),	51	51.2	vary	50.8	51
output Noise (dB) @3.4GHz	-195.5	-196.2	-194.8	-195.6	-193
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8
CMOS Technology(µm)	0.18	0.18	0.18	0.18	0.18

Table IX: PLL performance (transmission gate CP (path 1))

PLL parameters/Process corners (S1=0)	TT	SS	FF	FNSP	SNFP
Control voltage(V)	0.9	1	0.82	0.88	0.92
Max.Power(mW)	18.8	18.8	19.5	19.5	18.4
Pull-in time (ns)	295	480	190	240	315
Duty Cycle (%)	48.2	51	45.5	48.4	47.6

Max.Current(µA)	190	140	220	200	170
output Noise (dB) @3.4GHz	-195.5	-196.5	-194.3	-195	-166.4
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8

Table X: PLL performance (transmission gate CP (path 2))

PLL parameters/Process corners (S2=0)	TT	SS	FF	FNSP	SNFP
Control voltage(V)	0.9	1	0.82	0.88	0.92
Max. Power (mW)	18.8	18.8	19.5	19.5	18.4
Pull-in time (ns)	190	290	170	220	215
Duty Cycle (%)	48.2	52.5	45.2	48.1	48.2
Max. Current(µA)	220	170	270	250	220
output Noise (dB) @3.4GHz	-195.5	-196.3	-194.7	-195.2	-192
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8

Table XI: PLL performance (transmission gate CP (path 3))

PLL parameters/Process corners(S3=0)	TT	SS	FF	FNSP	SNFP
Control voltage(V)	0.9	1	0.82	0.88	0.92
Max. Power (mW)	19	18.9	18.6	19.5	18.4
Pull-in time (ns)	275	270	245	180	210
Duty Cycle (%)	48	52.3	45	48.1	47.8
Max. Current(µA)	300	220	380	300	280
output Noise (dB) @3.4GHz	-195.5	-196.3	-194.8	-195.2	-192.5
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8

Table XII: PLL performance (transmission gate CP (path 4))

PLL parameters/Process Corners (S4=0)	TT	SS	FF	FNSP	SNFP
Control voltage (V)	0.9	1	0.82	0.88	0.92
Max. Power (mW)	19.6	18.8	21.8	19.6	20
Pull-in time (ns)	not locked	420	not locked	390	not locked
Duty Cycle (%)	vary	52	vary	47.8	vary
Max. Current(µA)	430	350	550	450	500
output Noise (dB) @3.4GHz	-195.5	-166.4	-194.2	-195.5	-166.6
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8

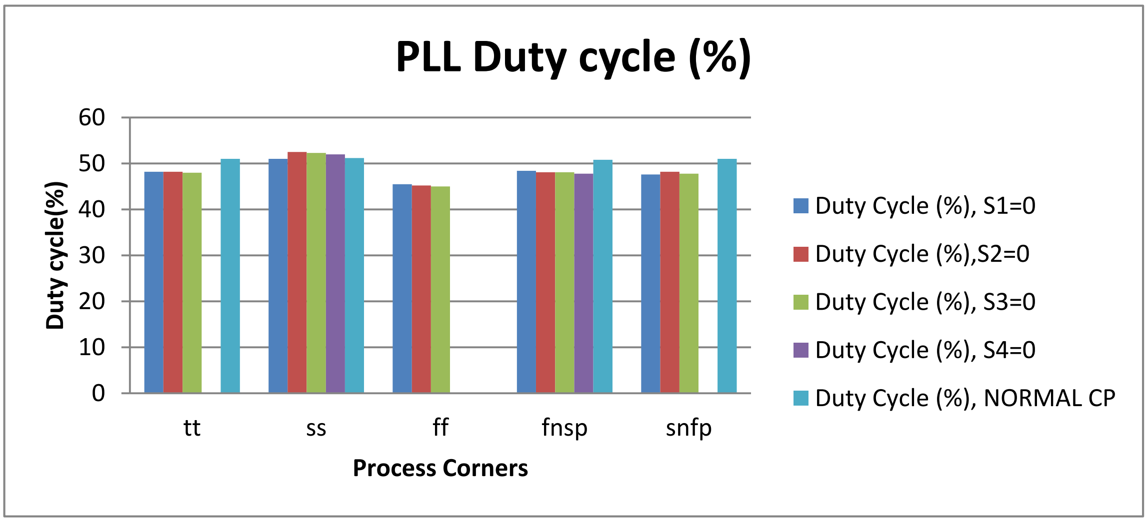

Fig25. PLL duty cycle versus Process corners

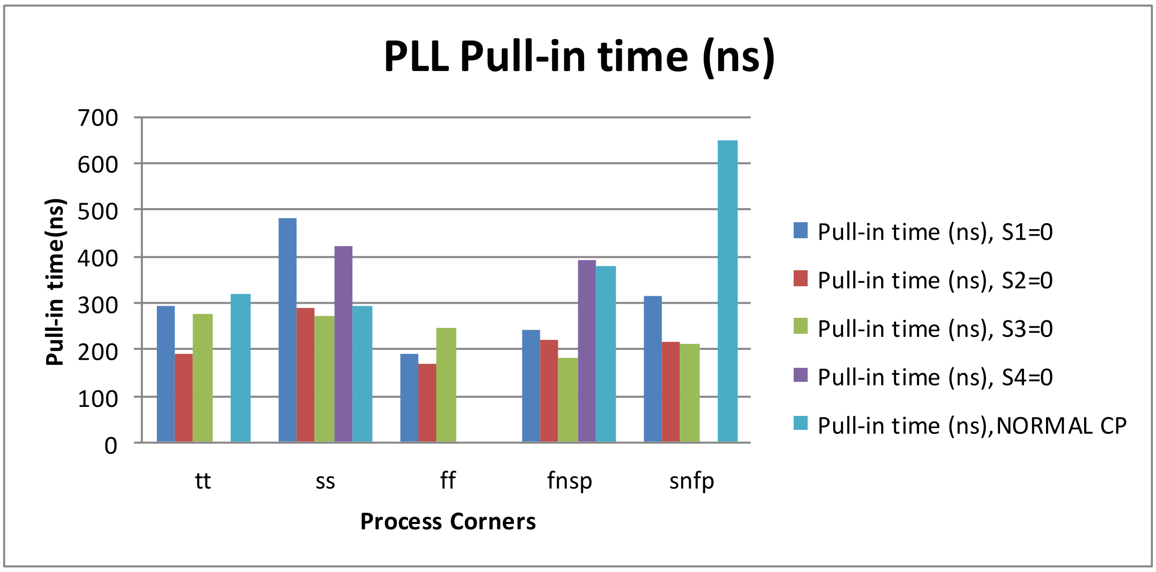

Fig26. PLL pull-in time versus Process corners

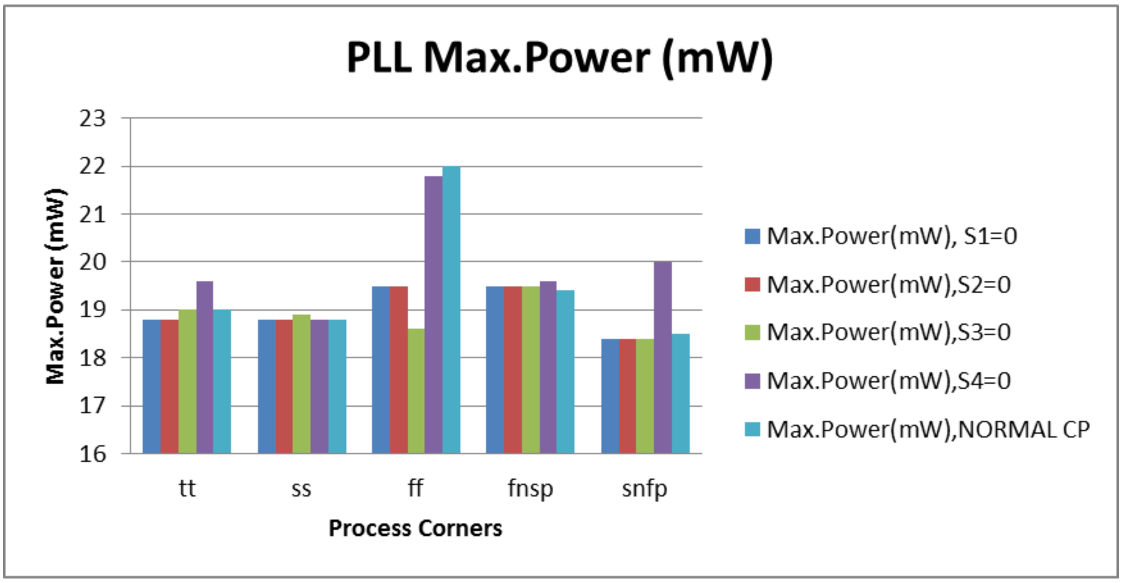

Fig27. PLL Max.power versus Process corners

V. CONCLUSION

The test data was generated by means of a 7-bit PRBS generator which used a 3.4 GHz clock signal provided by a Phase Locked Loop. The PLL block is designed to generate 3.4 GHz stable clock with low-jitter for HDMI applications which transfers data at the rate of 3.4 GB/s. All resistances and capacitances were extracted from layout such that we can simulate the circuits more accurately with post layout simulations. All transistors in the present design have been sized appropriately to achieve the targeted design. The proposed charge pump is designed by using Transmission gates with multiple current paths. By using this method a wide range of current is produced. Therefore a fast Pull-in time (Locking-time) for the PLL is observed. The overall jitter is decreased significantly. The rms jitter of this PLL is 1.18ps at 3.4GHz.The proposed PLL has been found to work under process-voltage-temperature (PVT) conditions (TT-1.8V-27°C, SS-1.7V-65°C, FF-1.9V-0°C). The PRBS and PLL Blocks are implemented with 1.8V, 0.18- µm CMOS Technology using Cadence-Virtuoso tool.

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