Single Transistor High-Impedance Tail Current Source With Extended Common-Mode Input Range and Reduced Supply Requirements

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***Abstract*—A compact implementation of a single transistor tail current source with very high output impedance (> 40 MΩ) and low-voltage requirements is introduced. The tail transistor can operate with less than a drain-source saturation voltage and allows implementation of low-voltage differential pairs with wide common-mode input range and very high common-mode rejection ratio. Simulation and experimental results are shown that validate the proposed circuit.**

***Index Terms*—CMOS analog integrated circuits, differential amplifiers, low-voltage analog circuits, operational amplifiers.**

I. Introduction

MODERN mixed-signal VLSI circuits operate from single supply voltages $V_{\rm DD}$ which are rapidly approaching sub-volt ($V_{\rm DD} < 1$ V) values. These low supply voltages are required to avoid gate oxide breakdown and to reduce power dissipation of the predominant digital circuitry (proportional to $V_{\rm DD}^2$). Low supply voltages leave very small headroom for signal swing in analog circuits, which requires new design strategies aimed at optimizing signal swing.

The most important building blocks of analog circuits are differential pairs and current mirrors. Mirrors with essentially reduced supply requirements and high performance characteristics have been reported recently [1]. The fact that input and output variables are in current form and internal voltages are compressed simplifies the design of low-voltage wide-swing current mirrors. However, differential pairs have voltage inputs complicating the achievement of large input swing. Fig. 1(a) shows a conventional differential pair biased by a tail current source I_B with output resistance $r_{\rm bias}$ and minimum required voltage across the current source $V_{\rm min}$. Ideally $V_{\rm min}$ should be small to increase the common-mode input range and $r_{\rm bias}$ should be very large to have high common-mode rejection ratio (CMRR). Unfortunately, cascoded current sources can increase $r_{\rm bias}$ but simultaneously increasing $V_{\rm min}$. If a single transistor M_B implements this current source [Fig. 1(b)] and we denote $V_{\rm DSsat}$ the minimum drain-source voltage to operate in saturation, then to keep all transistors in saturation $V_{\rm min} = V_{\rm DSsat}$ and the maximum input common-mode input signal range is $V_{\rm iCM}^{\rm MAX} = V_{\rm DD} - (V_{\rm GS} - V_{\rm min}) = V_{\rm DD} - (V_{\rm TH} + 2V_{\rm DSsat})$, where $V_{\rm TH}$ is the threshold voltage. Moreover, $r_{\rm bias} = r_{oB}$ (i.e., the output resistance of M_B), leading to a low ${\rm CMRR} = g_{m1,2} r_{\rm bias} = g_{m1,2} r_{oB}$ (on the order of 35–40 dB for $V_{{\rm DS},MB} > V_{\rm DSsat}$). For $V_{\rm TH} < V_{\rm iCM} < V_{\rm TH} + 2V_{\rm DSsat}$ the tail current source operates in triode mode, strongly degrading $r_{\rm bias}$ and thus CMRR. Using the cascode tail current source of Fig. 1(c) to increase $r_{\rm bias}$, then $r_{\rm bias} = r_{oB}(1 + g_{mC} r_{oC})$ and ${\rm CMRR} = g_{m1,2} r_{oB} (g_{mC} r_{oC})$ of about 70–80 dB are achieved. However, now $V_{\rm min} = 2V_{\rm DSsat}$ and $V_{\rm iCM}^{\rm MAX} = V_{\rm DD} - (V_{\rm TH} + 3V_{\rm DSsat})$. For instance, in a 0.18-μm CMOS technology with typical $V_{\rm DD} = 1.5$ V, $V_{\rm TH} = 0.5$ V and $V_{\rm DSsat} = 0.2$ V, $V_{\rm iCM}^{\rm MAX} = 0.4$ V, i.e., just 26% of the supply voltage. The CMRR can be increased even more using double or triple cascoded tail current sources, but further reduction in the common-mode input swing is experienced. To avoid this tradeoff between large $r_{\rm bias}$ and small $V_{\rm min}$ various solutions have been reported that use a single transistor tail current source [2]–[6]. In this brief, we present a new single transistor high-impedance tail current source with very simple architecture and low-voltage requirements (lower than $V_{\rm DSsat}$). The circuit is compared with these previous proposals, showing essentially lower supply requirements of the auxiliary control circuitry. Both simulations and experimental results are provided to verify the operation of the proposed circuit.

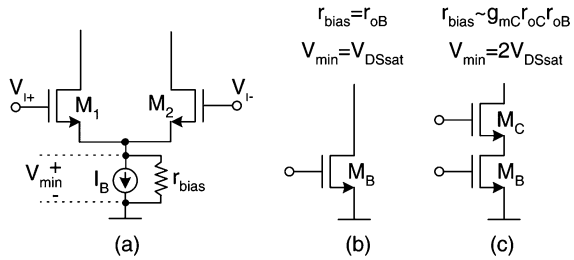

Fig. 1. (a) Differential pair. (b) Conventional single transistor tail current source (c) Cascode tail current source.

II. Previous Single-Transistor Tail Current Sources

Some techniques have been reported to increase the output impedance of the tail current source in Fig. 1(a) while using

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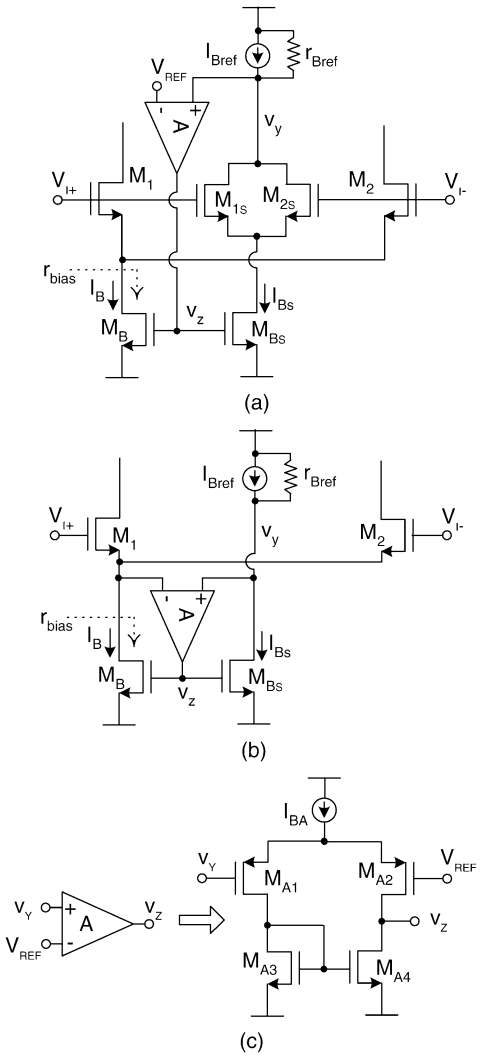

Fig. 2. Schemes of single transistor high-impedance low headroom tail current source. (a) Using auxiliary amplifier and a current sensing differential pair. (b) Using only differential auxiliary amplifier. (c) Implementation of auxiliary amplifier.

single transistor bias arrangements to preserve common-mode input swing. They are based on replica bias feedback circuits [2]–[6], and feature relatively high $r_{\rm bias}$ even in the transition region where the tail biasing transistor operates in triode mode. The approaches of [2]–[4] can be represented by the generic scheme of Fig. 2(a) which uses an additional differential pair (M_{1S}–M_{2S}) to sense and generate a replica I_{BS} of the bias current I_B in the main differential pair (M_1–M_2). Any nonzero incremental current difference $\Delta i = I_{BS} - I_{B\rm ref}$ generates an incremental voltage at the high-impedance node y $\Delta v_y = r_y \Delta i$ which is amplified and applied at node z (common gate of M_B and M_{BS}) according to $\Delta v_z = A r_y \Delta i$. This voltage modifies I_{BS} to compensate for the current error Δi. Assuming $I_{BS} = I_B$ the negative feedback loop formed by M_{BS}, M_{1S}–M_{2S} and amplifier A strive to maintain a constant tail current with value $I_B = I_{BS} = I_{B\rm ref}$ in M_1–M_2 and in M_{1S}–M_{2S}. In the circuit of Fig. 2(a), the output resistance of the tail current source is approximately $r_{\rm bias} = A r_{B\rm ref} A_{BS}$ where $A_{BS} = g_{mBS} r_{BS}$ is the voltage gain of M_{BS} (and M_B) and $r_{B\rm ref}$ the output resistance of $I_{B\rm ref}$. Gain A_{BS} is high (on the order of 50) for $V_{\rm DS} > V_{\rm DSsat}$ and drops (to unity or lower values) for $V_{\rm DS} < V_{\rm DSsat}$.

An alternative scheme for implementation of single transistor high-impedance tail current sources was reported in [5] and is shown in Fig. 2(b). It also uses an auxiliary differential amplifier that drives the gates of the tail current source transistor M_B and of a replica transistor M_{BS}. The amplifier in this case is used to equalize the $V_{\rm DS}$ of M_B and M_{BS} so that $I_B = I_{BS}$. In this scheme given that common-mode input voltage variations are transferred to the terminals of $I_{B\rm ref}$ it can be shown that $r_{\rm bias} = -r_{b\rm ref}$. Other schemes based on positive feedback have been reported to implement single transistor high-impedance tail current sources [6].

In the implementations of [3] and [4], the amplifier A is replaced by a straight connection so that $A = 1$ and $V_z = V_y = V_{{\rm GS},MB}$. The implementation of [4] includes also additional nMOS cascoding transistors in the main differential pair and between node "y" and the drains of M_{1S}, M_{2S}. They have both the drawback that high values for $r_{\rm bias}$ are maintained only over a relatively narrow range of common-mode input voltages: $V_{\rm GS} < V_{\rm iCM} < V_{\rm GS} + V_{\rm TH}$. For values $V_{\rm iCM} > V_{\rm GS} + V_{\rm TH}$ transistors M_{1S}, M_{2S} enter triode mode and feature $V_{\rm DS} < 0$ causing $r_{\rm bias}$ to decrease. Besides, increasing $V_{\rm DD}$ in these structures does not increase $V_{\rm iCM}^{\rm MAX}$. Another drawback of [3] and [4] (and [5]) is that large voltage variations are generated in V_z when M_B and M_{BS} enter triode mode. In this case $r_{\rm bias} = r_{B\rm ref}$. These variations are transferred to the terminals of the reference source $I_{B\rm ref}$. For this reason in order to maintain high impedance in the transition region $I_{B\rm ref}$ needs to be implemented as a cascoded (or double cascoded) source. The implementations of [2] and [5] use both auxiliary differential amplifiers A with a pMOS differential input stage [Fig. 2(c)]. The output terminal of A drives node z whose voltage increases rapidly (and approaches $V_{\rm DD}$) as M_B and M_{BS} enter triode mode. In both cases V_y must leave enough headroom for the differential pair in the auxiliary amplifier to remain functional. This sets a maximum value $V_{\rm REF}^{\rm MAX} = V_y^{\rm MAX} = V_{\rm DD} - (V_{\rm SGaux} + V_{\rm SDaux})$ and determines the maximum value for the common-mode input voltage that keeps M_{1S}, M_{2S} in saturated mode: $V_{\rm iCM}^{\rm MAX} = V_y^{\rm MAX} + V_{\rm THN} = V_{\rm DD} - 2|V_{\rm DSsat}|$.

III. Proposed Tail Current Sources

In order to overcome the limitations of [2]–[5] discussed above we propose the alternative simpler scheme of Fig. 3 in which A is implemented by a pMOS cascoding transistor $M_{\rm CP}$ connected between node z and node y. This corresponds to an auxiliary amplifier with gain $A = V_z/V_y = g_{mM\rm CP} r_{oM\rm CP}$ and with a dc level shift $V_{\rm SG}$. The voltage at node y is given by $V_y = V_{\rm CP} + V_{\rm SG}$. Voltage V_y can take values close to $V_{\rm DD}$ if $V_{\rm CP}$ has a value $V_{\rm CP} = V_{\rm DD} - V_{\rm SDsat} - V_{\rm SG}$. This selection allows $V_y^{\rm MAX} = V_{\rm DD} - |V_{\rm DSsat}|$. This implementation does not restrict the value of $V_{\rm iCM}$ in the positive direction, i.e., $V_{\rm iCM}$ can extend to the upper rail $V_{\rm iCM}^{\rm MAX} = V_{\rm DD}$. Hence, in this case, $V_{\rm iCM}^{\rm MAX}$ is not restricted to lower values by the load of the formerly employed differential pair.

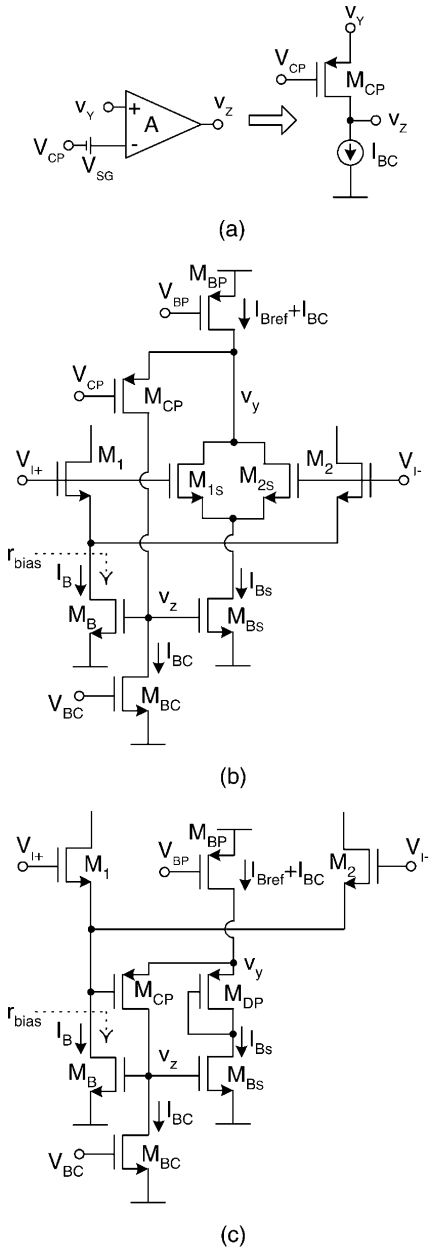

Fig. 3. (a) Implementation of auxiliary amplifier using cascode transistor. (b) Scheme of Fig. 2(a). (c) Scheme of Fig. 2(b).

In the proposed scheme $M_{\rm CP}$ acts simultaneously as auxiliary amplifier A and as cascoding transistor for the reference current source $M_{\rm BP}$. This leads to very small variations at the drain of $M_{\rm BP}$ as opposed to the schemes of [3]–[5]. In these former implementations, voltage across the terminals of $I_{B\rm ref}$ is subject to very large variations when M_B, M_{BS} enter triode mode.

Fig. 3(c) shows the utilization of a cascoding amplifier of Fig. 3(a) in the scheme of Fig. 2(a). In order to avoid a mismatch of value $V_{\rm SG}$ between the drain source voltages of M_B and M_{BS}, a diode-connected pMOS transistor $M_{\rm DP}$ has been included, thus achieving similar $V_{\rm DS}$ in M_B and M_{BS}. The output impedance in the implementation of Fig. 3(b) can be improved by including an additional pMOS cascoding transistor between $M_{\rm CP}$ and $M_{\rm BP}$.

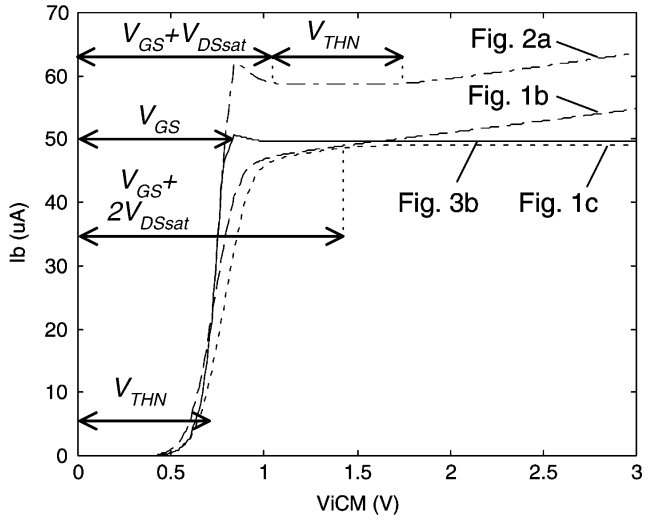

Fig. 4. DC transfer characteristics of the tail current in 1) Conventional DP of Fig. 1(a) using the single transistor of Fig. 1(b) and using the cascode of Fig. 1(c) 2) Circuit of Fig. 2(a) with $A = 1$, and 3) Circuit of Fig. 3(b).

IV. Simulation Results

The circuits of Fig. 1(a) [with current sources of Fig. 1(b) and (c)], Figs. 2(a) and 3(b) were simulated using 0.5-μm CMOS (MOSIS-AMI) technology parameters with nominal nMOS and pMOS threshold voltages $V_{\rm THN} = 0.73$ V and $V_{\rm THP} = -0.95$ V and with a single supply $V_{\rm DD} = 3$ V, $I_B = I_{B\rm ref} = 50$ μA, and following transistors sizes (in μm/μm):$W/L = 40/1.2(M_1, M_2, M_{1S}, M_{2S})$, $W/L = 80/1.2(M_B, M_{BS})$ and $W/L = 160/1.2(M_{\rm BP})$. Two 15-k$\Omega$ load resistors are used in the differential pairs. Fig. 4 shows the tail current of M_1, M_2 as a function of the common-mode input voltage $V_{\rm iCM}$ applied at the gates of M_1, M_2, M_{1S}, M_{2S} for following four cases: 1) The conventional differential pair of Fig. 1(a) with the current source of Fig. 1(b); 2) The same differential pair of Fig. 1(a) but with the cascode current source of Fig. 1(c); 3) The circuit of Fig. 2(b) with a straight connection from node z to node y (this corresponds to the implementations of [2]–[4] with $A = 1$); and 4) the proposed implementation of Fig. 3(b) (solid line). It can be seen that, as expected, the output impedance of the proposed implementation remains very high ($\sim$ 40 MΩ) for a wide common-mode input range $V_{\rm GS} < V_{\rm iCM} < V_{\rm DD}$. The output impedance of the implementation of [3] is high ($\sim$ 2 MΩ) but only over a relatively limited range $V_{\rm GS} < V_{\rm iCM} < V_{\rm GS} + V_{\rm TH}$. The proposed differential pair and the implementation of [3] turn fully on (off) within a narrow range of common-mode input voltages of width $V_{\rm DSsat}$ (for $V_{\rm TH} < V_{\rm iCM} < V_{\rm TH} + V_{\rm DSsat}$) while the conventional differential pair in its simple (or cascoded version) turn on gradually over wider input common-mode range of width 2 $V_{\rm DSsat}$ (3 $V_{\rm DSsat}$ for the cascoded version). Once they are fully on with their transistors in saturated mode the conventional differential pair has a moderately high output resistance $r_{\rm bias} = r_o(\sim 50$ k$\Omega)$ for $V_{\rm iCM} > V_{\rm GS} + V_{\rm DSsat}$ and the cascoded version has a high $r_{\rm bias} = r_o g_{mC} r_{oC} (\sim 3$ M$\Omega)$ for $V_{\rm iCM} > V_{\rm GS} + 2V_{\rm DSsat}$, with $V_{\rm GS} = 0.9$ V, $V_{\rm DSsat} = 0.2$ V and $V_{\rm TH} = 0.7$ V.

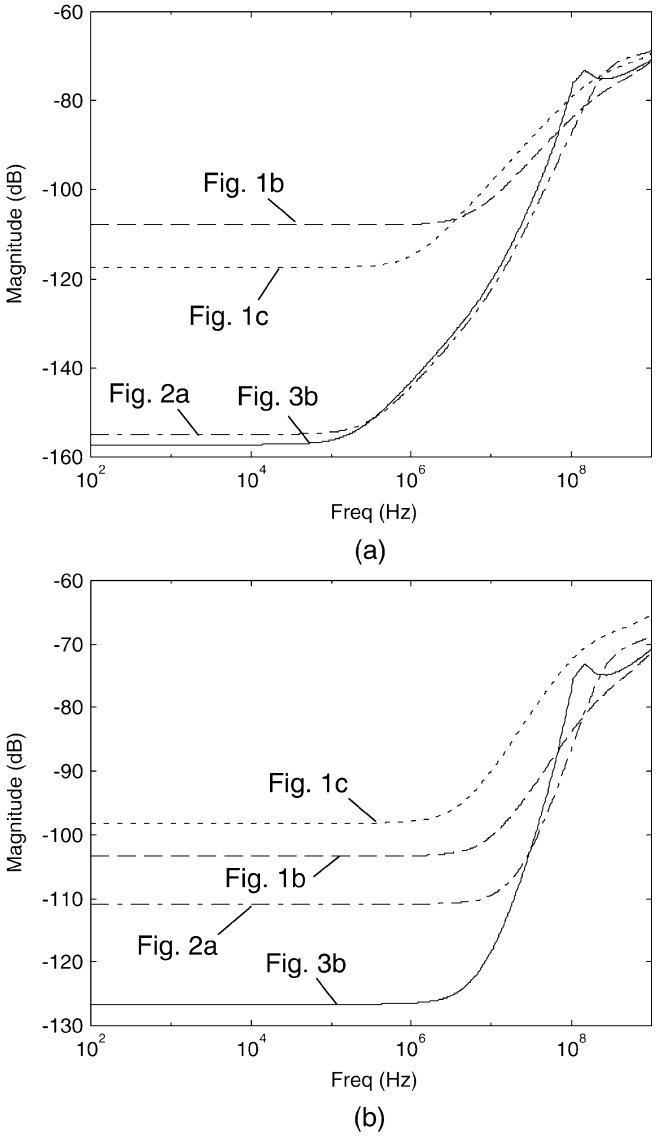

Fig. 5. Simulated ac common-mode transconductance gain for 1) Conventional DP of Fig. 1(a) using the single transistor of Fig. 1(b) and using the cascode of Fig. 1(c) 2) Circuit of Fig. 2(a), $A = 1$, and 3) Circuit of Fig. 3(b). (a) $V_{\rm iCM} = 1.3$ V, (b) $V_{\rm iCM} = 1.1$ V.

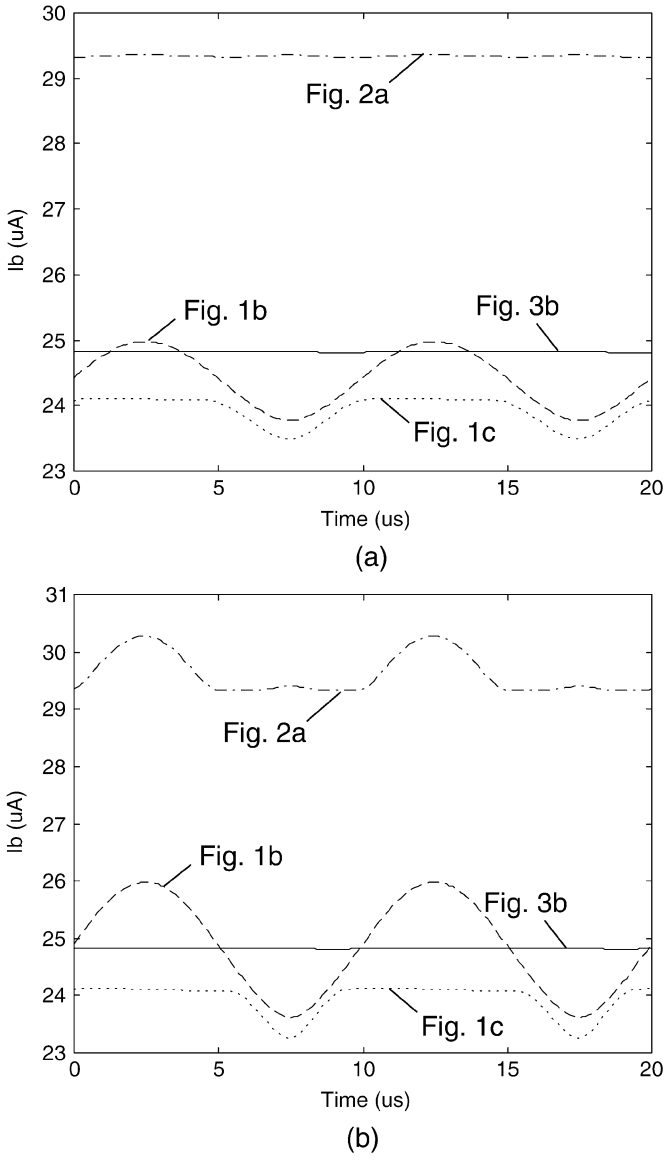

Fig. 6. Simulated transient drain currents $I_{D1,2}$ for 100-kHz input common-mode signal and 1) Conventional DP of Fig. 1(a) using the single transistor of Fig. 1(b) and using the cascode of Fig. 1(c) 2) Circuit of Fig. 2(a) with $A = 1$, and 3) Circuit of Fig. 3(b) (a) $V_{\rm iCM} = 1.4$ V and input common-mode amplitude 0.3-V peak. (b) $V_{\rm iCM} = 1.65$ V and input common-mode amplitude 0.6-V peak.

Fig. 5 shows the ac responses of the common-mode drain currents in the same four cases considered above and for two different common-mode input voltages: In Fig. 5(a) the common-mode input voltage is $V_{\rm iCM} = V_{\rm GS} + V_{\rm DSsat} = 1.3$ V and in this case the tail current sources of all circuits operate in saturation. In Fig. 5(b), the input common-mode voltage has a value $V_{\rm iCM} = V_{\rm GS} = 1.1$ V and it is selected so that the tail current sources M_B and M_{BS} operate in triode mode. Note how the proposed implementation shows improved rejection of common-mode signals.

Fig. 6 shows the transient response of the drain currents $I_{D1} = I_{D2}$ for the same four cases in Fig. 4 by application of a 100-kHz input common-mode voltage signal with [Fig. 6(a)] 0.3-V peak amplitude superimposed on a 1.4-V dc component. It can be seen that due to the relatively low output impedances and the fact that both the conventional and the conventional cascode differential pairs of Fig. 1 enter their transitions regions (where tail sources operate in triode mode) large common-mode tail current variations can be observed. In the proposed circuit and in the circuit of [3] (that remains in its high-impedance region) very small variations can be observed in Fig. 6(a) while in Fig. 6(b) relatively large variations can be seen in all cases exception made of the proposed circuit Fig. 3(b). This is due to the fact that the tail source in the circuit of [3] and in the conventional differential pairs leave the high-impedance region.

V. Experimental Results

Breadboard prototypes of the circuits of Figs. 1, 2(a), and 3(b) were built using commercial integrated precision matched transistor arrays ALD1106 and ALD1107. These are characterized by transconductance gain factors and threshold voltages $\beta_{\rm nMOS} = 180\ \mu$A/V^2, $V_{\rm TH}^{\rm nMOS} = 0.75$ V and

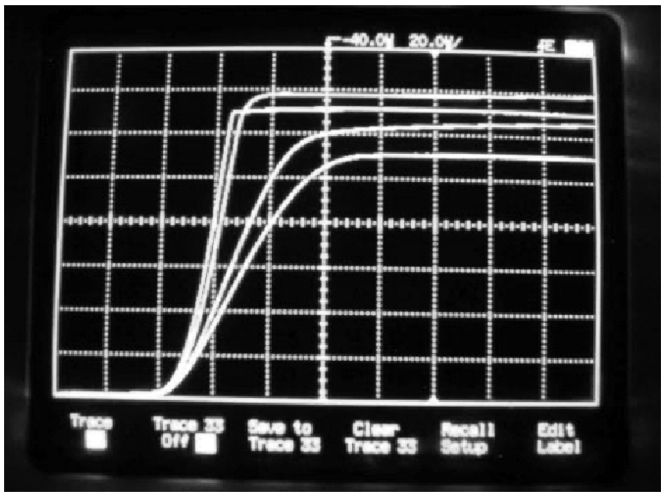

Fig. 7. Experimental plot of drain currents in M1, M2 versus common-mode input voltage for: a) Conventional cascode DP (bottom trace), b) conventional (third trace from top to bottom), c) proposed circuit of Fig. 3(b) (second trace from top to bottom) and d) circuit of Fig. 3(b) with $A = 1$ (top trace). Horizontal axis: 0.3 V/div, Vertical axis 8 μA/div.

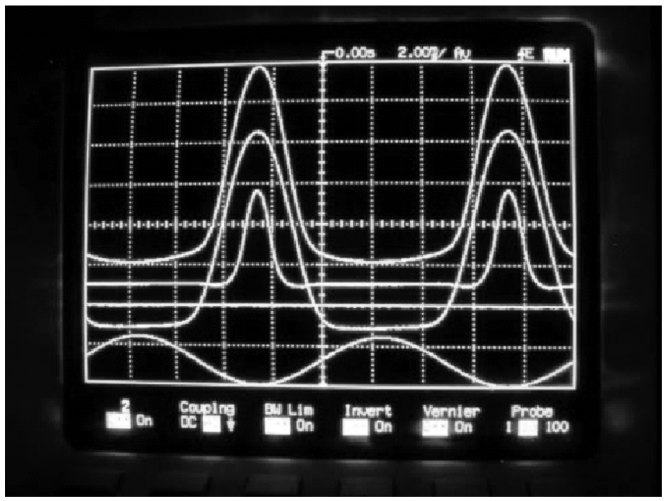

Fig. 8. Experimental transient drain voltage waveforms in M_1, M_2 for 0.6-V_{pp} sinusoidal common input signal (bottom waveform): Conventional DP (top trace), circuit of Fig. 2(a) with $A = 1$ (second trace from top to bottom) proposed circuit of Fig. 3(b) (third trace from top to bottom) and conventional cascode DP (fourth trace from top to bottom). Horizontal axis: 2 μs/div, Vertical axis 50 mV/div on 15-kΩ load resistor (equiv. to 3.3 μA/div). $V_{iCM} = 1.6$ V and 1.1-V_{pp} input sinusoidal waveform.

$\beta_{pMOS} = 40\ \mu$A/V^2, $V_{TH}^{pMOS} = -0.75$ V, and channel-length modulation parameters $\lambda_{nMOS} = \lambda_{pMOS} = 0.03$ V^{-1}, respectively. A single supply $V_{DD} = 3$ V, a bias current $I_B = 60\ \mu$A, and 15-kΩ load resistors were used to test the circuits. Fig. 7 shows the experimental characterization of the drain currents versus the common-mode input voltage V_{iCM} for the same four cases considered in Fig. 4. It can be seen that there is very good agreement between these curves and the simulation results of Fig. 4. Fig. 8 show the transient voltage waveforms response at the drain of M_1, M_2 for the same four cases of Fig. 6 upon application of a 1.1 V_{pp} 100-kHz sinusoidal common-mode input signal with a superimposed dc component $V_{iCM} = 1.6$ V. Large voltage (current) variations can be seen in the conventional and cascode conventional differential pair due to the fact that they both leave their high-impedance regions. However, in the other two cases very small current variations can be seen. Notice that the waveforms of Fig. 8 are inverted with respect to those of Fig. 6 given that drain voltage waveforms $V_{DM1,2}$ are related to the drain current waveforms $I_{DM1,2}$ by the load resistance R_L according to $V_{DM1,2} = V_{DD} - R_L I_{DM1,2}$. These results validate experimentally the proposed circuits.

VI. Conclusion

A new compact implementation of a high-impedance single transistor tail current source based on replica bias feedback was introduced. It operates with drain source voltages lower than V_{DSsat} and with higher output impedance than a conventional source. Simulations and experimental results were shown that verify its operation. It can be used for the implementation of differential pairs with reduced supply headroom, high CMRR and extended common-mode input range.

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