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Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials

Revija za mikroelektroniko, elektronske sestavne dele in materiale

Dear

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Editorial board of the Journal Informacije MIDEM chose you to act as a reviewer of the sent article. Based on your judgement the board will decide whether to publish or refuse the contribution. Please, return the form giving also written opinion about the contribution.
We are expecting your answer within 14 days.

Uredništvo revije " Informacije MIDEM " Vas je izbralo za recenzenta priloženega prispevka. Na osnovi Vašega mnenja se bo uredništvo odločilo za objavo ali zavrnitev prispevka. Prosim, poleg obrazca podajte tudi pismeno mnenje o prispevku.
PROSIM ZA STROKOVNO RECENZIJO ČLANKA V ROKU 14 DNI PO PREJETJU.

Author :	**Title :**
Xiaofeng Wang, Zhiyu Wang, Haoming Li, Rongqian Tian, Jiarui Liu, and Faxin Yu	An Improved Low Phase Noise LC-VCO with Wide Frequency Tuning Range Used in CPPLL

Editor-in-chief
Ljubljana : Marko Topič:

REVIEW POINTS

(*MERILA ZA RECENZIJO)*

	YES	NO	Partially
Is the contribution content appropriate for publishing? *Ali je prispevek dovolj tehten in vsebinsko primeren za objavo ?*	X		
Is the content on the appropriate scientific level? *Ali je vsebina na ustrezni znanstveno strokovni ravni ?*	X		
Has the contribution been published in the same or similar form before ? where? *Ali je bil material že objavljen v takšni ali podobni obliki ? Kje ?*			X
Is the contribution prepared according to instructions for authors? *Ali je prispevek napisan in opremljen v skladu z navodili za avtorje ?*	X		
Is data reliable and documents the findings appropriately ? *Ali so podatki zanesljivi in zadostno dokumentirajo ugotovitve ?*	X		

REVIEWER'S EXPLANATION :

OBRAZLOŽITEV RECENZENTA :

(1) When MOS transistors of either polarity are used in analog circuits, the connection of the substrate is not trivial. Please use appropriate transistor symbols including the substrate. See enclosed drawing.
(2) What is the 1/f-noise corner frequency of your MOS transistors? It seems that your equation [3] does not account for 1/f-noise that may be quite high in MOS transistors. Why do you not use the complete Leeson's equation that accounts for all noise sources?
(3)What is the exact switch design for the capacitor bank. What are the gate widths of the different transistors in the oscillaor and in the capacitor bank.
(4) Fig.7 only shows a section of your chip with no bonding pads. Which circuits do you have on the same chip? How do you decouple the digital-circuitry noise from modulating the analog VCO?
(5) On Fig.8(b) you only plot the output phase noise of a locked PLL. What is the phase-noise performance of a free-running VCO?

SUGGESTIONS TO THE EDITORIAL BOARD:

PREDLOGI UREDNIŠTVU :

- ◊ The contribution can be accepted as original scientific work (prispevek lahko sprejmete kot izvirno *znanstveno delo*)
- ◊ The contribution can be accepted as professional work (prispevek lahko sprejmete kot strokovno delo)
- ◊ The contribution can be accepted as an overview work (prispevek lahko sprejmete kot pregledno delo)
- ◊ The contribution can be accepted after corrections (prispevek lahko sprejmete po popravkih) Minor!
- ◊ the contribution is to be rejected (prispevek zavrnite)

Reviewer (*Recenzijo opravil*)	Date (*datum*) :
Matjaž Vidmar	05.08.2017