A 11mW 2.4GHz 0.18 μm CMOS Transceivers for Short-Range Communications

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Abstract In this paper, a low power transceiver for short range communications is proposed. Targeting the applications in Internet-of-Things (IoT), the system is designed with fully functional blocks including a receiver, a Fractional-N frequency synthesizer, and a Class-E transmitter, and it is optimized with a good balance among performances such as power consumption, silicon area, sensitivity and output power. A TX-RX shared input-output matching network is used so that only one off-chip inductor is used in the system. The power and area efficiency oriented fully-integrated frequency synthesizer is able to provide programmable output frequencies at 2.4GHz range while occupying a very small silicon area. Implemented in a standard 0.18 μm RF CMOS technology, the whole transceiver occupies a chip area of 0.5 mm^2 (1.2 mm^2 including bonding pads for QFN package). Measurement results suggest that the design is able to work at OOK and FSK modes with up to 200 kbps data rate. With an input sensitivity of -60dBm and an output power of 4 dBm, the receiver, transmitter and frequency synthesizer consumes 2.3mW, 4.8mW and 3.9mW from a 1.8 V supply voltage respectively.

1 Introduction

Short-distance communications have recently spurred lots of researches and developments. The RF transceiver is undoubtedly one of the key components in a communication system[1-5]. However, it is not possible to design a transceiver for all kinds of communication systems. Depending on the applications, the topologies of transceivers may vary considerably in terms of the system architecture and performances such as data-rate, power consumption, silicon area [1-10]. For example, CMOS RF transceivers for short-range communications have been reported extensively, it is still of a great importance to design transceivers for certain applications since no one solution can cover all the desires in different scenarios where the design strategies may vary significantly. To achieve ultra-low power

consumption, many transceivers are designed without low noise amplifier (LNA) or voltage controlled oscillator (VCO)[4][10]. Such a topology exhibits a poor functionality though. For an oscillator-less design or injection-locked oscillator based architecture, e.g., the transceivers are unable to provide programmable channel frequencies, enhance only one frequency channel is supported and the system is very sensible to in-band interferences. The applications of such a system are quite limited even the sub-mW operation is achieved [10]. In the applications of IoT, the design considerations are quite different even a low power consumption is always a key advantage. The amount of chips used in the IoT applications will be massive, and there are many different protocols and communication standards involved in such applications, it is highly desired that the transceiver is designed with fully functional blocks such as LNA, PLL, and the cost of the circuits should be as low as possible. For example, the design will be attractive if all the circuits can be implemented with low cost but reliable technology such 0.18 μm CMOS technology which maintains a well balance among level of integration, cost, performances[11]. Of course, the designs should be of less off-chip components and small silicon area. Therefore, the on-chip inductor or large capacitor (higher than pF) should be kept as less as possible.

By considering all these factors, this paper presents a low power transceiver working on the 2.4GHz band which is one of the most popular ISM communication bands. The system is designed with conventional architecture but it is optimized to maintain a well balance among the considerations in IoT applications. This paper is organized as follows: Section 2 presents the system planning of proposed transceiver, followed by the implementation of circuits in Section 3. Section 4 demonstrates the experimental results of the proposed circuits and system, while Section 5 is the conclusion.

2   System-level design of a short-range transceiver

The architecture of a transceiver greatly depends on the applications of system. For short range applications, the data rate and the distance of signal transferring are quite limited, hence the key considerations are low power consumption and small silicon area (low cost). The link budget as well as the sensitivity of the receiver are given by [4].

$$P_{RX,in} = P_{TX,out} - 20\log(4d\pi/\lambda) \tag{1}$$

$$Sens_{RX} = NoiseFloor + 10\log BW + NF + SNR_{out} \tag{2}$$

Where $P_{TX,out}$ is the output power of the transmitter, d is the distance of communication, λ is the wave length of the carrier. Since the distance of communication is at metre level, a lower output power of PA or received power of RX is possible. As illustrated in [4], at the distance within one metre, even a -40dBm received power is possible with 40GHz carrier. The requirement of received power can be even relaxed for a 2.4GHz carrier which is with much less attenuation of propagation. Moreover, as shown in equation 2, for a fixed noise floor, to accommodate a lower data rate transferring, it is possible to use a narrow signal bandwidth and a simpler modulation scheme, this makes a poor sensitivity or noise figure acceptable in the transceiver.

Fig. 1 shows the architecture of the proposed system. It includes three key sub-systems,

namely the receiver(RX), phase-locked loop (PLL), and transmitter (TX). The receiver includes a low noise amplifier, mixer, low pass filter with amplifier stage (IF amplifier) and the buffer for test proposal. The local oscillator (LO) signal is provided by a PLL, which includes a crystal driver as the reference clock, a phase-frequency detector (PFD), charge pump (CP), loop filter, voltage controlled oscillator (VCO) and a Fractional-N divider. The output signal of the PLL is also used as the input signal of power amplifier (PA) after a buffer stage, which generate Frequency Shift Keying (FSK) or Amplitude shift keying (ASK)/on-off-keying (OOK) output signals of the TX. The target performances of this system are determined as follows based on the above mentioned strategy.
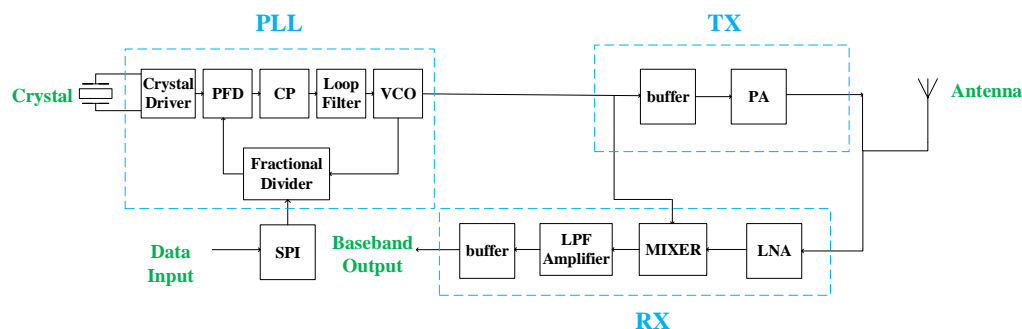

Fig. 1 The architecture of the proposed work

The system is designed using a 0.18μm CMOS technology, which is a popular solution for nowadays industrial applications. For simplicity, the transceiver is designed to support FSK and ASK system since the requirement of data-rate is quite low (usually considerably lower than 1Mbps) in a typical IoT system. If more complex modulation schemes are needed, digital baseband system can be added in the proposed work. The specifications of the subsystem can be determined based on the operating frequency and technology in use since many individual building blocks has been reported in literatures [12]. In this scenario, the maximum noise figure of the receiver can be as high as 20dB[12]. This makes it possible to achieve a low power consumption in the design of RX (mW level). At the distance of around 10 metres, the output power of 0 dBm or less is a reasonable choice, even higher output power is possible in CMOS technology [11]. For a power amplifier with a power efficiency of 20%, the DC power consumption of a TX will be less than 5mW[12]. To improve the performance, accurate LO is needed even the requirement of phase noise performance is not a tough one. For example, -96dBc/Hz @1MHz-offset will be enough in such a system[12].

3 Circuit Implementation
    3.1 Low noise amplifier and power amplifier
    Fig. 2 shows the topology of the low noise amplifier and the power amplifier. It is an inductor reuse topology proposed in [12]. As mentioned above, the key considerations in this transceiver are low cost (small silicon area) and flexibility in functionality subject to acceptable performances such as noise figure, gain and linearity. Hence it is necessary to maintain less off-chip component and small silicon area. Also it would be more attractive if the transceiver is able to be re-configured for different applications since the IoT applications cover a wide range of operating frequencies. So the strategy in this design is that the RX and

TX are inductor-less and only one off-chip inductor is shared by RX and TX. The silicon area of the transceiver will therefore be ultra-small. Moreover, since the matching network is determined by the inductor and capacitor, it will be very convenient to make the RX and TX working properly at desired frequency range.

a)   b)

Fig. 2 Topology of the LNA and PA a) low noise amplifier b) PA with control circuit

As illustrated in [12], since the TX and RX share an antenna, the PA and LNA can be co-designed to share matching network. The basic consideration is that when the LNA is at off-mode, the system is working as a transmitter. However, the LNA simultaneously contributes parasitic capacitance. Similarly, at the RX mode when the PA is powered off, the parasitic capacitance of the PA should be included in the simulation of LNA.

The PA in this design is a conventional Class-E topology as shown in Fig. 2. It consists of three stages of inverters, the output stage has an output matching network with an on-chip capacitance and an off-chip inductor with capacitances, which forms a PI-matching topology. This topology, which is widely used in short range communication exhibits a high efficiency and small silicon area. Also, the external matching network make it possible to re-configure the system at different working frequencies.

Similarly, the LNA is designed to maintain a good balance among the required performances. To achieve a wide operating band, a common gate topology is implemented since a higher noise figure is acceptable in this system. The parallel resonant circuit shared with the power amplifier forms a band-pass frequency response which improves the robustness against interferences. Another important trade-off is the load of the amplifier. A resistive instead of commonly use inductive load is implemented in this design to achieve small silicon area. The drawback of this design is lower high frequency gain, sizing of the transistors and resistors is carried out to ensure acceptance performances in noise figure, gain and linearity at desired operating frequency.

Fig. 3 shows the simulation results of the low noise amplifier. It has a wide-band of gain performance, which is over 12 dB from several hundred MHz to 3GHz. The noise figure of the LNA is about 6-7 dB within the band of interest. The performances are quite acceptable for a receiver with a noise figure budget up to 20dB. The lP3 of the amplifier, as shown in Fig. 4, is higher than 0dBm, which suggests that the RX exhibits a good linearity.
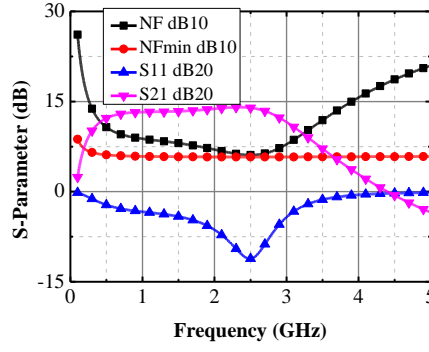
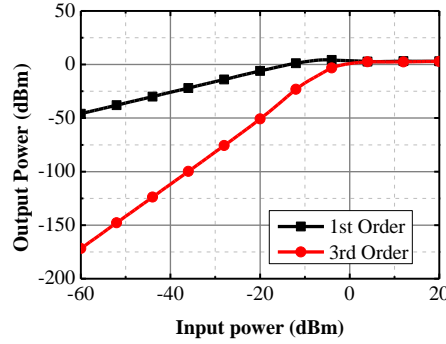Fig. 3. The simulated S parameters and noise figure of the LNA

Fig. 4 The simulated IP3 of the low noise amplifier

3.2 Mixer and analogue baseband circuits

Since the low noise amplifier is single-ended, a single balanced active mixer is used to save power. The topology in this design quite conventional and the major task here is to proper sizing of these devices to achieve a low power consumption subject to acceptable gain and linearity (Noise figure of active mixer is not an issue compared with passive one). The gain of the mixer linearly proportional to the trans-conductance of the transistor *NM2/NM3* and the reload resistance of the mixer. To save power consumption, it is desirable to use a larger resistance such as 6K Ohm in this work. Using the biasing current of 0.6mA, it is possible to achieve over 300mV output swing and over 15dB gain at 2.4GHz to 2.5MHz (IF) gain. For the linearity, it is mainly decided by the biasing condition of the MOS transistor.

a)   b)

Figure 5. The mixer a) topology b) simulated gain

With regarding to the low data in this work, the IF frequency is set to 2.5 MHz (reconfigurable). The signal is amplified with an IF amplifier with programmable gain control. The design is a conventional MOS switch based amplifier [13]. By controlling the biasing condition and switching of different loads. The amplifier has tuning range of 30dB in gain.

3.3 Frequency synthesizer

The frequency synthesizer has been a major bottleneck of fully-integrated transceiver [14-15]. Due to this large silicon area and power consumption, it is usually an off-chip sub-system in many ultra-low power solutions. However, in this work, to ensure robustness and maximized flexibility, it is designed as a fully-integrated subsystem which frequency outputs fractional to reference clocks. It includes a voltage-controlled oscillator, a Fractional-N frequency divider, a phase-frequency detector, a charge pump and a loop filter as shown in Fig. 1.

The voltage controlled oscillator is the key building block in term of working range, phase noises, output power of the PLL. The key considerations are acceptable phase noise with low power consumption and small silicon area. To improve the power efficiency, the PMOS-NMOS cross-coupled negative-G_m LC oscillator is used as shown in Fig. 6. The optimization is mainly focused on the high-performance LC tank. The oscillator has a start-up condition which is determined by the quality of the tank and the negative G_m to compensate the tank loss, which suggests that a low power is only possible for a high-Q tank. At 2.4GHz range, the low quality factor of inductor is the major concern. A high Q can be obtained using an off-chip inductor, but it is sensible to additional parasitic effects in package and PCB. In this work, properly sizing of this on-chip fully symmetrical inductor is carried to ensure a high quality factor (around 10) at desired frequency range. The overall quality factor of the LC tank is about 6-7. After optimization, the biasing current of 0.7mA is able to ensure a robust operation of the oscillator (3 times higher than the start-up condition in G_m). In additional to the varactors for continuous frequency tuning, a 3-bit digitally controlled capacitance bank is implemented so that the proposed VCO can work properly from 2.2GHz to 2.6GHz. The gain of the VCO (K_{VCO}) is designed to be about 120 MHz/V to maintain a good phase noise performance, while covering the 2.4GHz operating bands with certain redundancy. Thanks to this PMOS-NMOS cross-coupled topology, the output power of this VCO is around 3 dBm, which is large enough for the proper operation of the down conversion mixer in the receiver. As shown in Fig. 7, the simulated phase noise of the VCO is -113 dBc/Hz at 1 MHz offset.
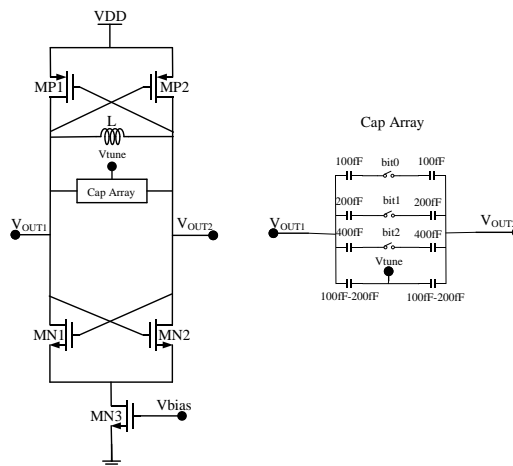
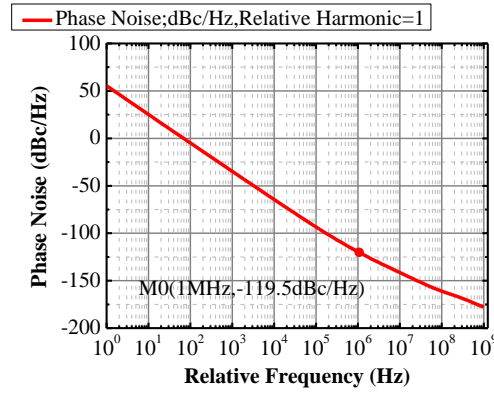Fig. 6 The topology of the VCO

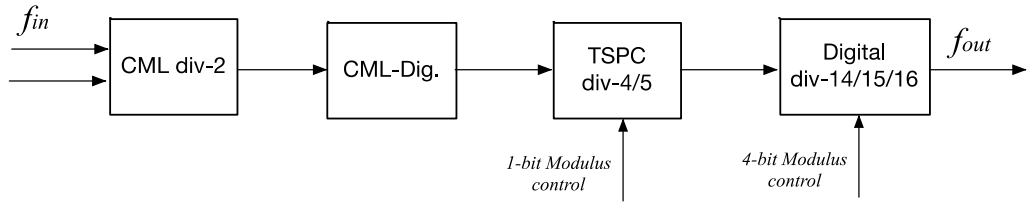Fig. 7 Simulated phase noise of the VCO

Fig. 8 The frequency divider

Another key building block is the frequency divider. As shown in Fig. 8, It includes a divide-by-2 prescaler, a divide-by-4/5 prescaler, the P counter with division ratio of 14, 15, 16. The total division ratio is 2x(52+M), where is M is fractional number, which is controlled by a 10-bit sigma-delta modulator (Configured in Mash 1-1-1). The most important optimization is the power consumption[14]. In this work, the blocks in the frequency divider are designed to be power efficient at the certain work frequencies. The prescaler is most challenging building block in the frequency divider since it works at the highest operating frequency. The MOS current mode logic (MCML) is the most popular solution at the operating frequency above GHz. However, it is quite power consuming compared with dynamic digital logic such as true-single-phase-clock (TSPC). In this work, to maintain a good balance between operating frequency and power consumption, the input signal is firstly divided by 2 using a MCML divider followed by a differential-to-single-ended buffer (CML-Dig. in Fig. 8). Since the output frequency is now about 1.2GHz, it is possible to use more power efficient logic, namely the TSPC logic in the following divide-by-4/5 prescaler. Similarly, the output of the divide-by-4/5 prescaler is less than 400MHz so the following frequency division can be performed by the divide-by-14/15/16 counter implemented using standard static CMOS logic, which is stable and easy to implement. The total division ratios are determined by four bits of modulus control signals, which are connected to a sigma-delta modulator. In this system, the modulator is of three stages (in Mash 1-1-1) each of which is a 10-bit configuration. In this work, the total division ratio is set to be (2×(52+M)), where M is a programmable fraction number. Using this Fractional-N topology, it is able to achieve division ratios which is in a fractional instead of integer number. And it is now possible to use a higher reference clocks for the PLL system, which results in fast settling time and maximized functionality.

The other building blocks in the PLL, as shown in Fig. 9, are quite conventional. The PFD is a dead zone free digital detector and the charge-pump (CP) is a conventional one as shown in Fig. 9. The charge current is about 100 µA. A 3rd order RC based loop-filter is used for better suppression of the reference spurs. In this work, key consideration is the capacitor should be small enough to have a fully-integration solution. The parameters of the components in the loop filter is determined by the closed-loop transfer function of the PLL [Perrot]. The whole PLL system is now a 4-order system [13]. Since the gain of the VCO frequency tuning, operating frequency, division ratio, and charge current have been determined, the PLL has the freedom in optimization of loop filters. As the key target is the silicon area which is occupied by the loop capacitor. In this design, the maximum capacitance after optimization is 1.4 pF, which ensure a small silicon area in fabrication.

Fig. 9 The topology of PFD, CP and loop filter

Simulation of the PLL is carried out using Cadence Spectre RF at transistor-level in a 0.18 µm CMOS technology (post-layout). Simulation suggests that the proposed PLL is able to work at 2.4GHz with less 20 µs settling time as shown in Fig. 10.
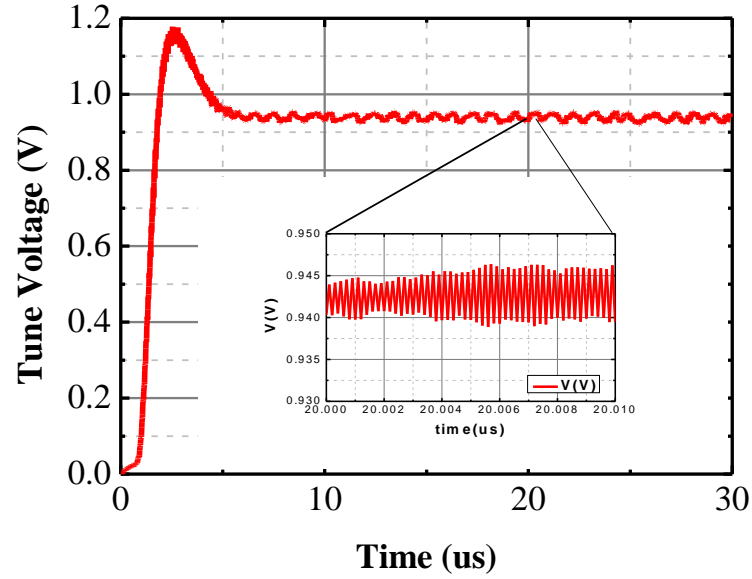
Fig. 10 The schematic level simulation result of the PLL

3.4 System level integration

Besides the key building blocks, there are also some other circuits in the proposed system. The most important part is Serial Peripheral Interface (SPI) circuit since many circuits in the system are configurable. For example, the transceiver can be configured as RX or TX and the gain of the RX is programmable. In addition, by changing the division ratios, which is equal to $2\times(52+M)$, the output frequency of the PLL is configurable to support different channels. Accordingly, the working bands of the voltage controlled oscillator should be adjusted to support the desired operating frequencies. By designing SPI circuit, all the control bits can be set by several on-chip registers.

Finally, as a complete chip, it includes some functional building blocks such as the biasing circuits, crystal buffer and decoupling capacitors. The crystal buffer is designed to support an off-chip crystal of 20MHz (to meet 2.4GHz PLL output frequency range). De-coupling capacitors between supply voltage and ground are added as many as possible to improve the noise performance. Implemented using a 0.18 μm CMOS technology, the layout of the transceiver is about $0.7\times0.7mm^2$ and the fully chip is about $1.1\times1.1mm^2$ in adding the capacitors and ESD pads.

4. Measurement results

The proposed transceiver is fabricated using a 0.18 μm CMOS technology. Fig. 11 shows the die photo of the transceiver, which is packaged in a QFN 24 form for measurement proposal.
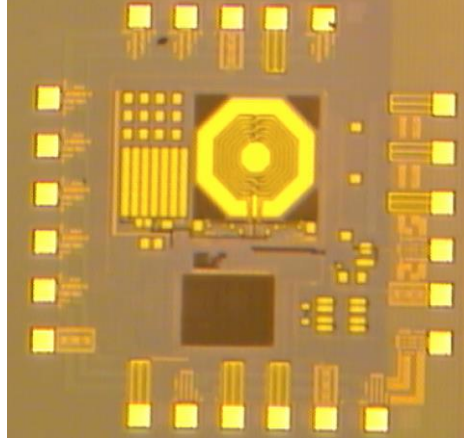
Fig. 11 The die photo of the proposed transceiver

The first step of measurement is to set up the initial status of SPI with determines the working conditions of the circuits. For example, the phase-locked loop of this chip. The frequency of the locked PLL is determined by the integer tuning bits (Ch1-0, D11 and D10 of the SPI register) and fractional tuning bits (F9-0, D21 to D12 of the SPI register) of the PLL. The output frequency of the PLL, f_{out} is given by:

$$f_{out} = (59 + Ch1\text{-}0 + F9\text{-}0/1024) \times 2 \times 20MHz \qquad (3)$$

For proper operation of the PLL, one needs to tune the coarse frequency bits of the VCO manually, namely D2-D0 of the SPI register (maybe with the help of a spectrum analyser). The VCO free running frequency should be close to the targeted 2.4-2.5GHz range.

The matching network for the RFIO port is as follows. The inductance value can be from 2.5 to 3 nH. In this work, the LNA and PA share the matching network with a port namely RFIO.
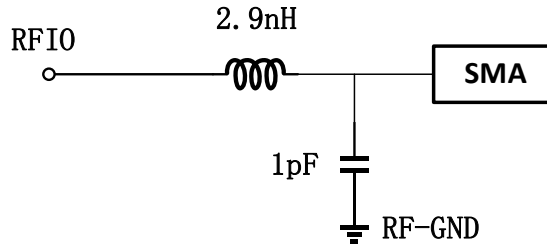

Fig. 12 The off-chip matching network of RFIO

The reference clock of the PLL is 20MHz, which comes from off-chip crystal. With the three-bit control of VCO working bands, the PLL can work from 2.2GHz to 2.5GHz properly. Fig. 13 shows the output spectrum of the PLL working at 2.5GHz range.
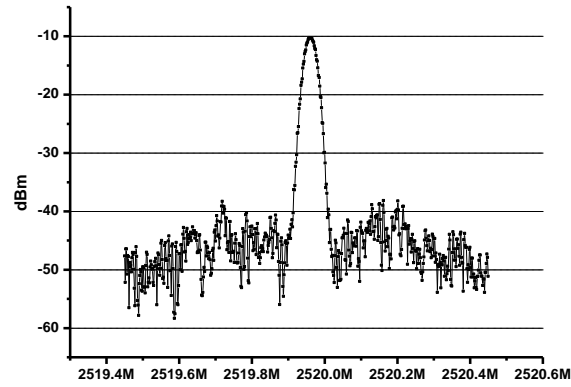
Fig 13. Output spectrum of the PLL

As mentioned above, the transceiver supports the working mode of FSK, which is achieved by the changing output frequency in the PLL. The output spectrum of this working mode is shown in Fig. 14.
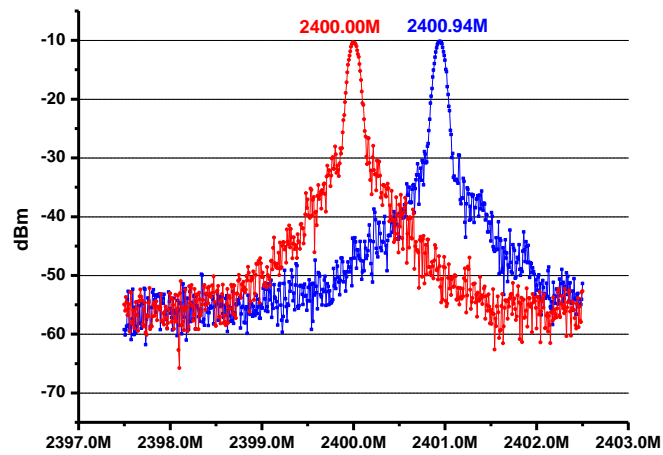

Fig. 14. An example of FSK output spectrum

After the verification of local oscillator, it is possible to connect the output of the PLL to PA, which generator the output of ASK or FSK signal. Fig. 15 shows the output spectrum of the PA.
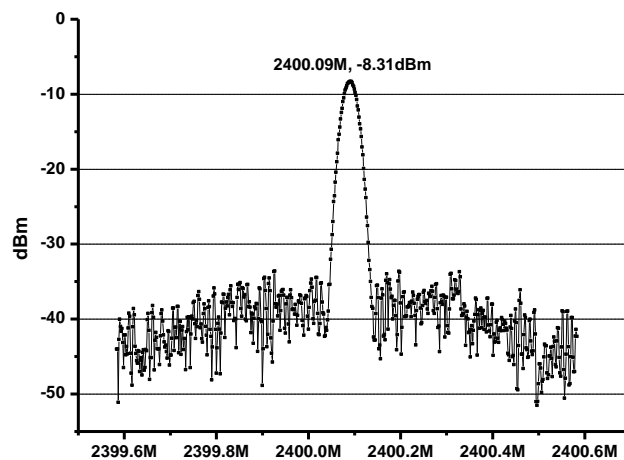

Fig. 15. Output spectrum of the PA

Finally, this signal is received by the RX, which generate the IF signal at around 2.5MHz (depending on the configuration). The IF amplifier has 25dB tunable gain to support the dynamic range of the RX.
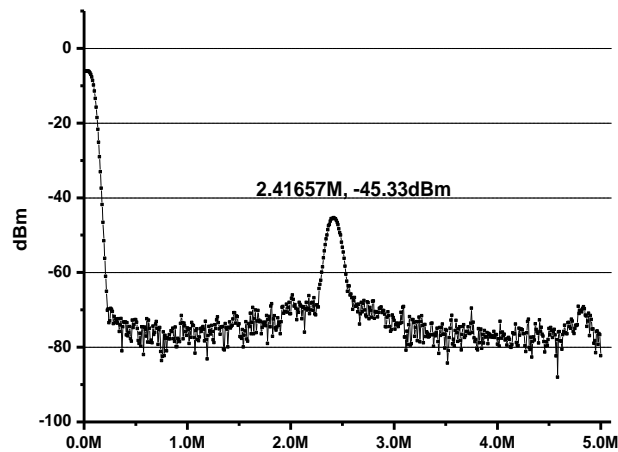

Fig. 16. IF signal of the RX

Based this analogue performance measurement, it is possible to measure the transceiver using digital signals. Different data patterns of 0001_1111_0101_1011_0111_1100 are used in the transceiver. Fig. 17 shows the output data of TX (red) and the IF signal of RX (blue) respectively.
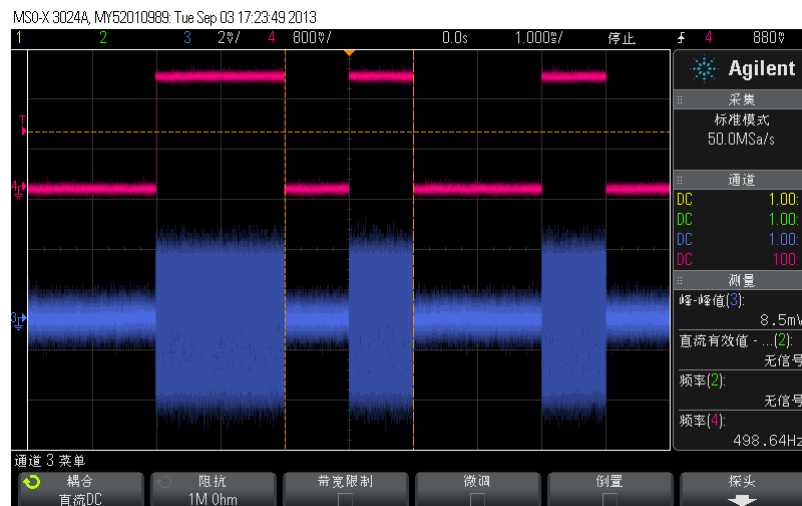

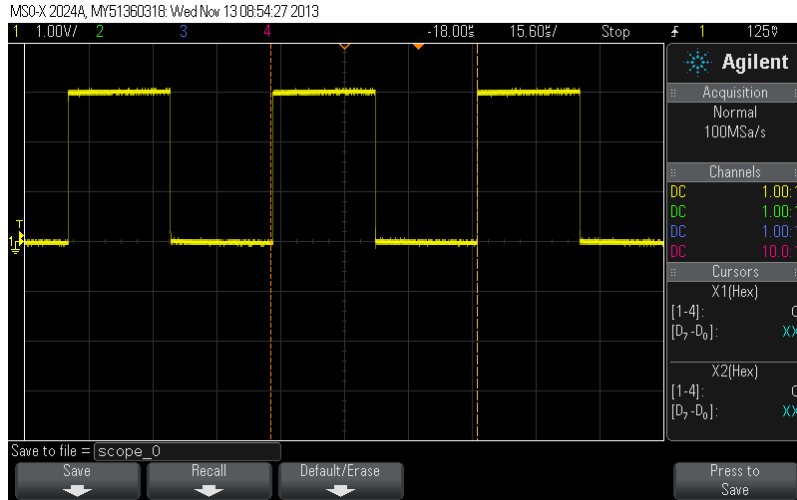Fig 17. Data in TX (red) and IF in RX (blue)

Fig. 18 The recovered data signal

By using a FSK demodulator or a compared at the output IF signal, the data signal can be easily recovered as shown in Fig. 18. Measurement results suggest that the proposed transceiver is able to work with 500Kbps data transferring with mW level power consumption. Table I compared the proposed work with some of the recent literatures in similar technology. It is not of the lowest power efficient, but it is based on the standard architecture with a large flexibility in system performances and it can be easily changed to different applications. Thanks to the low cost CMOS technology with small silicon area (only one external inductor needed), it is of a great interest in the applications of IoT.

Table I Comparison of proposed work with literatures

Transceiver			
Reference	[3]	[8]	This Work
Technology	0.18 μm	0.18 μm	0.18 μm
Supply	1.8	1.8V	1.8V
Modulation	N/A	QPSK	FSK/OOK
Frequency	2.4	2.4	2.4
Data rate	N/A	2Mbps	500Kbps
Power consumption	49.3mW	17mW	11mW
Silicon area	3.92 mm^2	2.85 mm^2	1.2 mm^2 (0.7 w/o pads)

5 Conclusion

This paper presents a low cost 2.4GHz CMOS transceiver. An input-output matching network is share by LNA and PA to save silicon and simplify the topology. Power consumption optimization is carried out in phase-locked loop to maintain a good balance among phase noise and working range. Implemented in a standard 0.18 μm CMOS technology, the proposed work is able to work 2.4GHz with 500K bps transferring rate, while consumption 11mW from a 1.8V supply voltage.

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