An improved BPSK demodulator for the 1.2Mbit/s packet-radio RTX

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1. PSK demodulator design and performance

Efficient data transmission requires efficient modulation and demodulation techniques, both for terrestrial radio links and for satellite communications. Unfortunately, most amateur transmissions still use rather inefficient FSK modulation. Although an incoherent FM transceiver may look simpler than a coherent PSK transceiver, the practical implementation of either design is equally demanding.

Coherent PSK becomes really necessary at data rates above about 100kbit/s, where the power and spectral inefficiency of incoherent FSK severely limits the performance even for short-range terrestrial links. The simplest form of coherent PSK is Bi-phase PSK or BPSK. The latter is very suitable for amateur packet-radio links.

Coherent BPSK was successfully tested already a few years ago in 1.2Mbit/s packet-radio links as described in [1]. The only disadvantage were relatively complicated 13cm BPSK transceivers, as described in [3] or [5]. In fact only the double-conversion 13cm BPSK receiver is complicated and requires lots of shielding and a complicated tuning procedure. On the other hand, it is always possible to design a direct-modulation BPSK transmitter without any frequency conversions or other complicated signal processing.

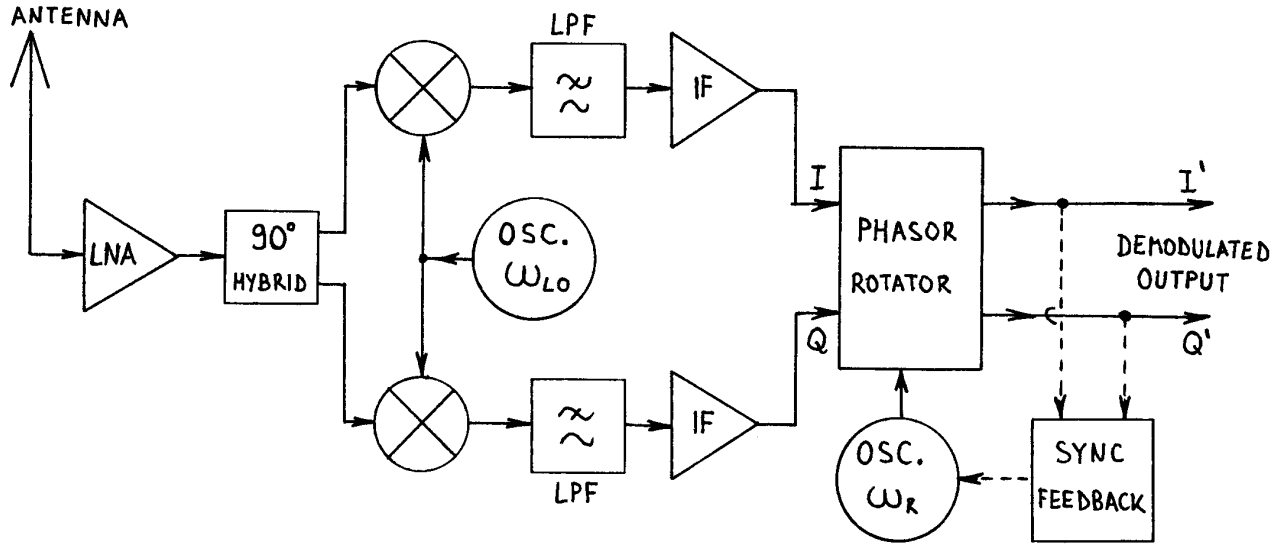


Figure 1 - Zero-IF receiver block diagram.

The receiver radio-frequency hardware can be much simplified using a Zero-IF design as shown on figure 1. On the other hand, a Zero-IF receiver requires more complex IF signal processing. Since the latter is performed at relatively low frequencies, it only requires simple and inexpensive hardware. BPSK or QPSK demodulation simply requires an additional phasor rotation to compensate for the frequency and phase offset of the receiver local oscillator.

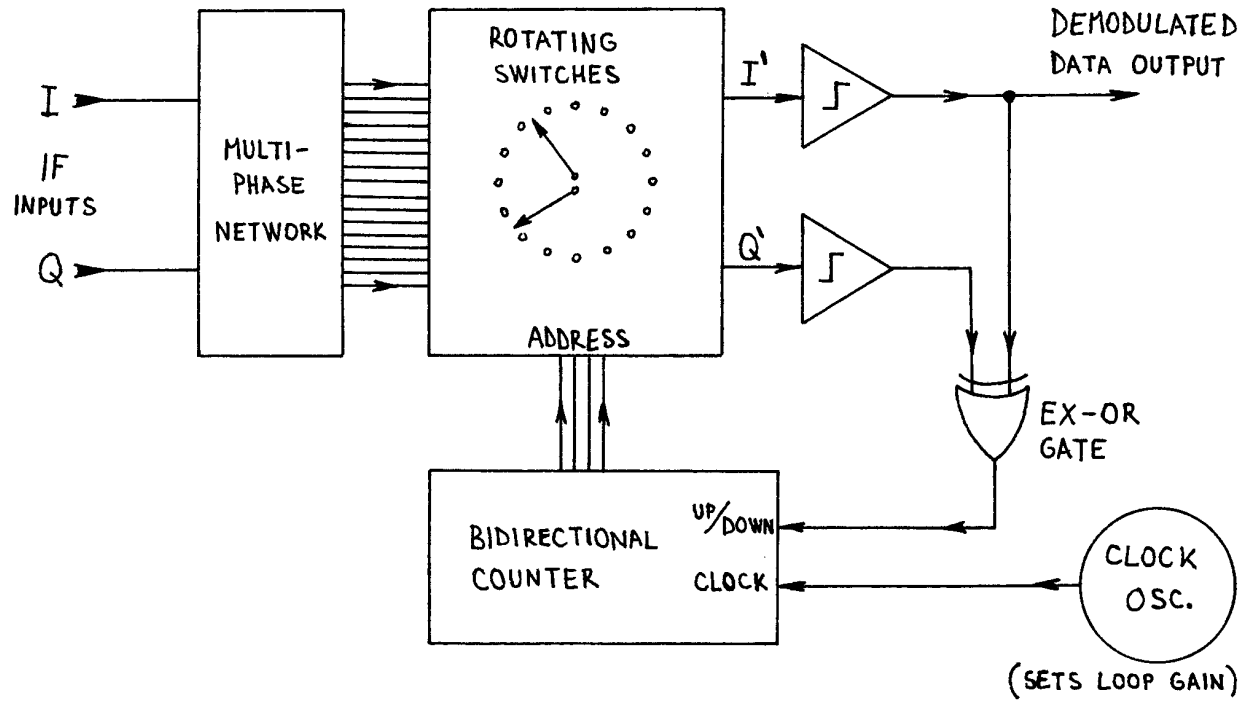


Figure 2 - Costas-loop BPSK demodulator with rotating switches.

A very successful 23cm Zero-IF BPSK transceiver design for 1.2Mbit/s was presented in [2], [4], [6] or [7]. This transceiver uses a Costas-loop BPSK demodulator. The phasor rotation is achieved with a pair of rotating, analog CMOS switches, while the feedback loop is built as a digital PLL, as shown on figure 2. This design results in inexpensive and highly reproducible hardware with no tuning points.

The measured bit-error rate performance of the described demodulator is compared to the theoretical performance of a BPSK demodulator on figure 3. The performance loss amounts to about 3...4dB and has many sources. About 0.7dB loss is caused by rotating the phasor in 16 discrete steps instead of a continuous phase adjustment. Less-than-ideal IF filtering accounts for at least 1dB of performance loss.

Additional performance loss is caused by the switching transients caused by the analog CMOS switches and the non-ideal IF frequency response: the IQ dual IF amplifier can not be DC coupled for many practical reasons. The effects of the latter are particularly noticeable with longer pseudo-random test sequences.

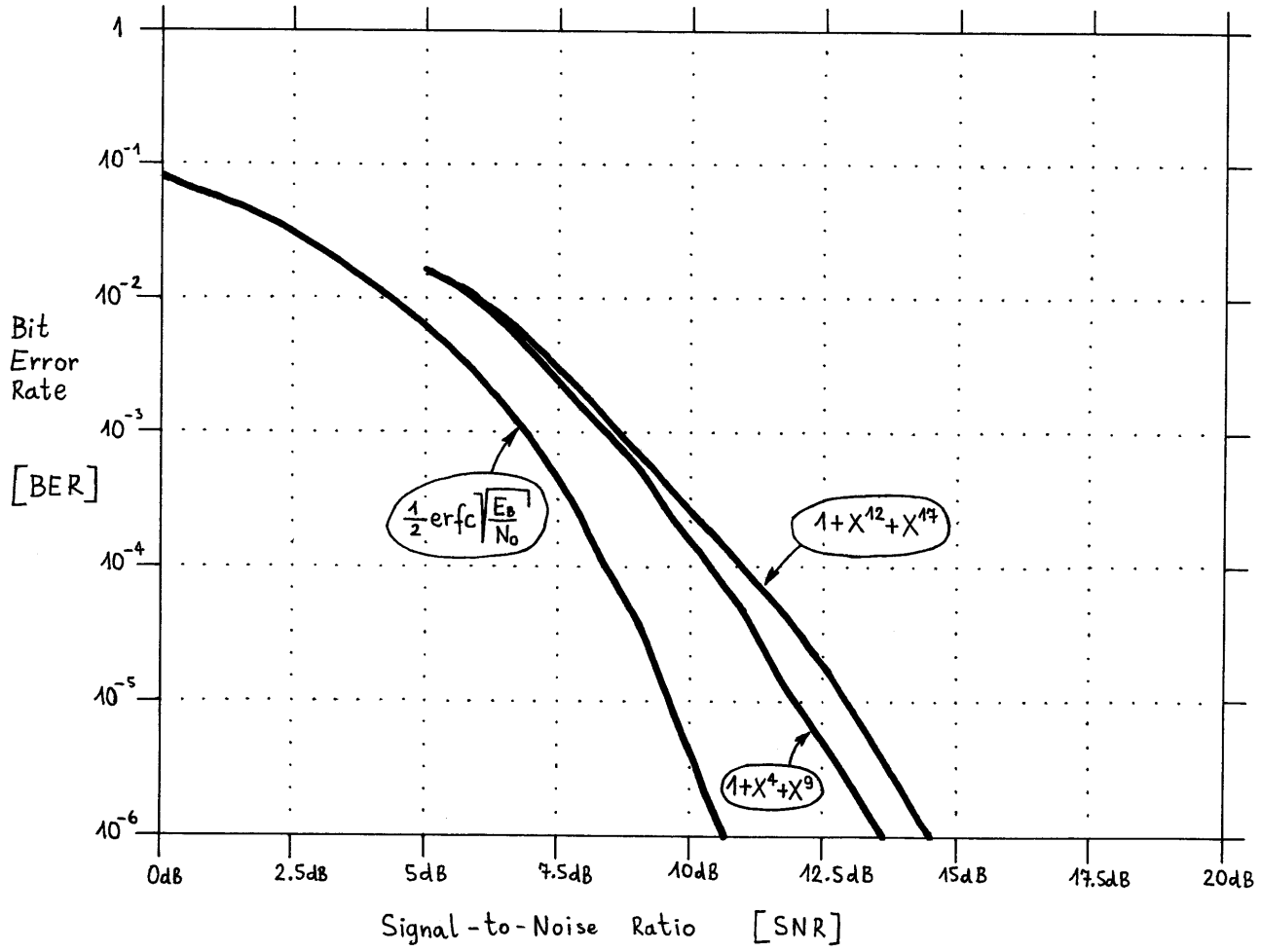


Figure 3 - Measured BPSK demodulator performance.

With long test sequences, the performance of the demodulator may be even worse than shown on figure 3 in the particular case when the receiver LO frequency matches the transmitter frequency within a few kHz. In this particular case, the rotating switches toggle between two neighbor positions most of the time thus increasing the effects of switching glitches. The IF signal itself includes an increased DC component, corrupted by the AC-coupled dual IF amplifier.

In this article, an improved BPSK demodulator is described that is completely compatible with the 23cm BPSK transceiver from [2], [4], [6] or [7]. The new demodulator completely solves the problem of switching transients and requires a lower gain IF amplifier, thus reducing the signal distortion. Finally, the new demodulator actually requires less components resulting in a simpler and cheaper circuit.

2. Improved BPSK demodulator

The operation of the new BPSK demodulator is also based on a phasor rotator with rotating switches with a block diagram similar to figure 2. The main difference from figure 2 is that the multiphase network drives a number of limiting amplifiers. The rotating switches are digital selectors and the switching transients can be removed easily with D-flip-flops.

A phasor rotation in 16 discrete steps requires 16 limiting amplifiers and 16-position switches. The actual hardware can be much simplified by considering that the second group of 8 limiting amplifiers provides just an inverted replica of the signals from the first group of 8 limiting amplifiers. Therefore just 8 limiting amplifiers are required in the practical implementation, followed by 8-position switches and finally EXOR gates to flip the phase of the signals when required.

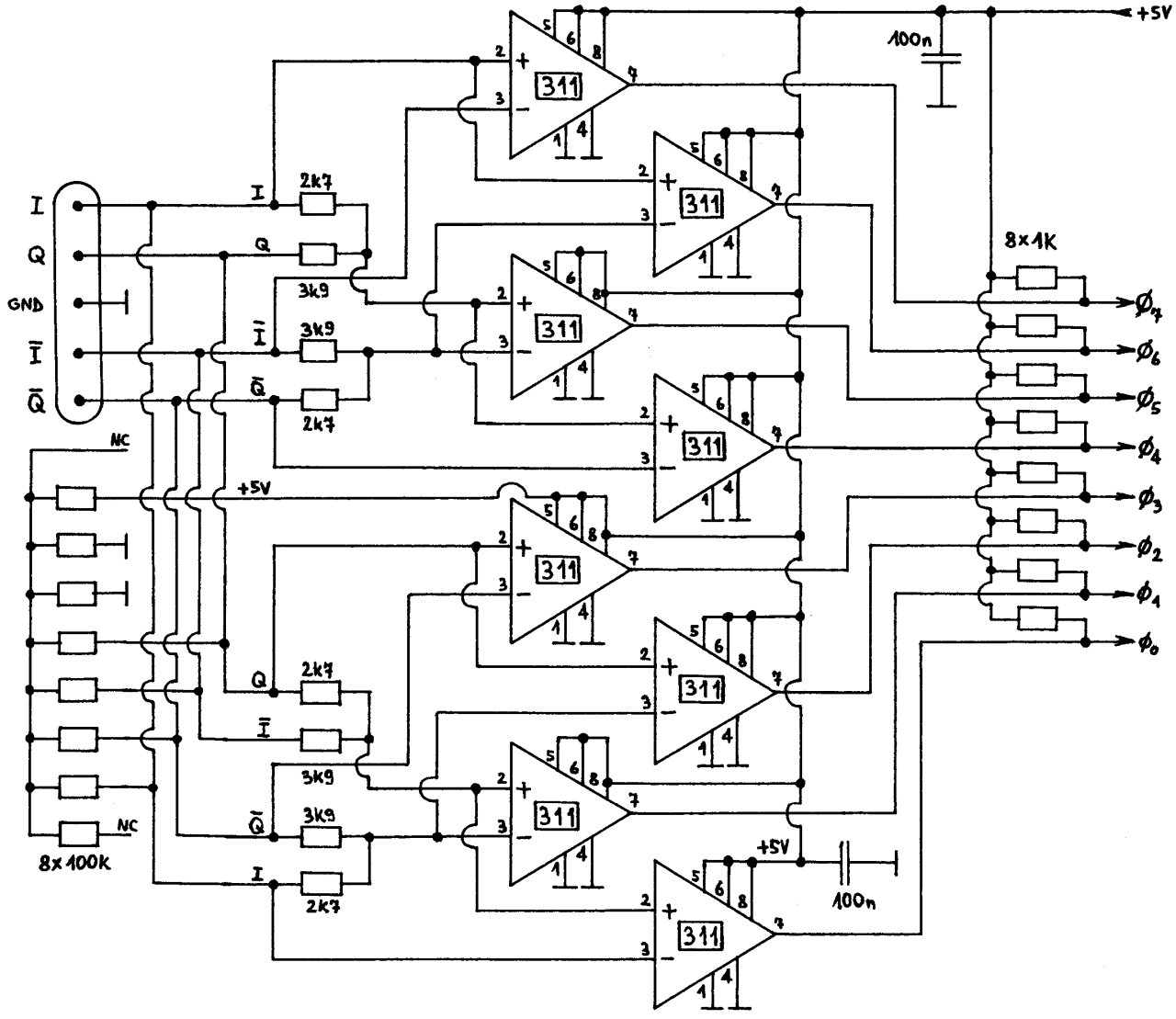


Figure 4 - Analog part of the demodulator: 8-phase limiting IF.

The analog part of the new BPSK demodulator is shown on figure 4. The IF signals I and Q and their inverted replicas, AC coupled from the dual IF amplifier,

drive a resistor network. Eight LM311 comparators are used as limiting amplifiers. Taps on the resistor network are selected to obtain eight signals with phases of 0, 22.5, 45, 67.5, 90, 112.5, 135 and 157.5 degrees.

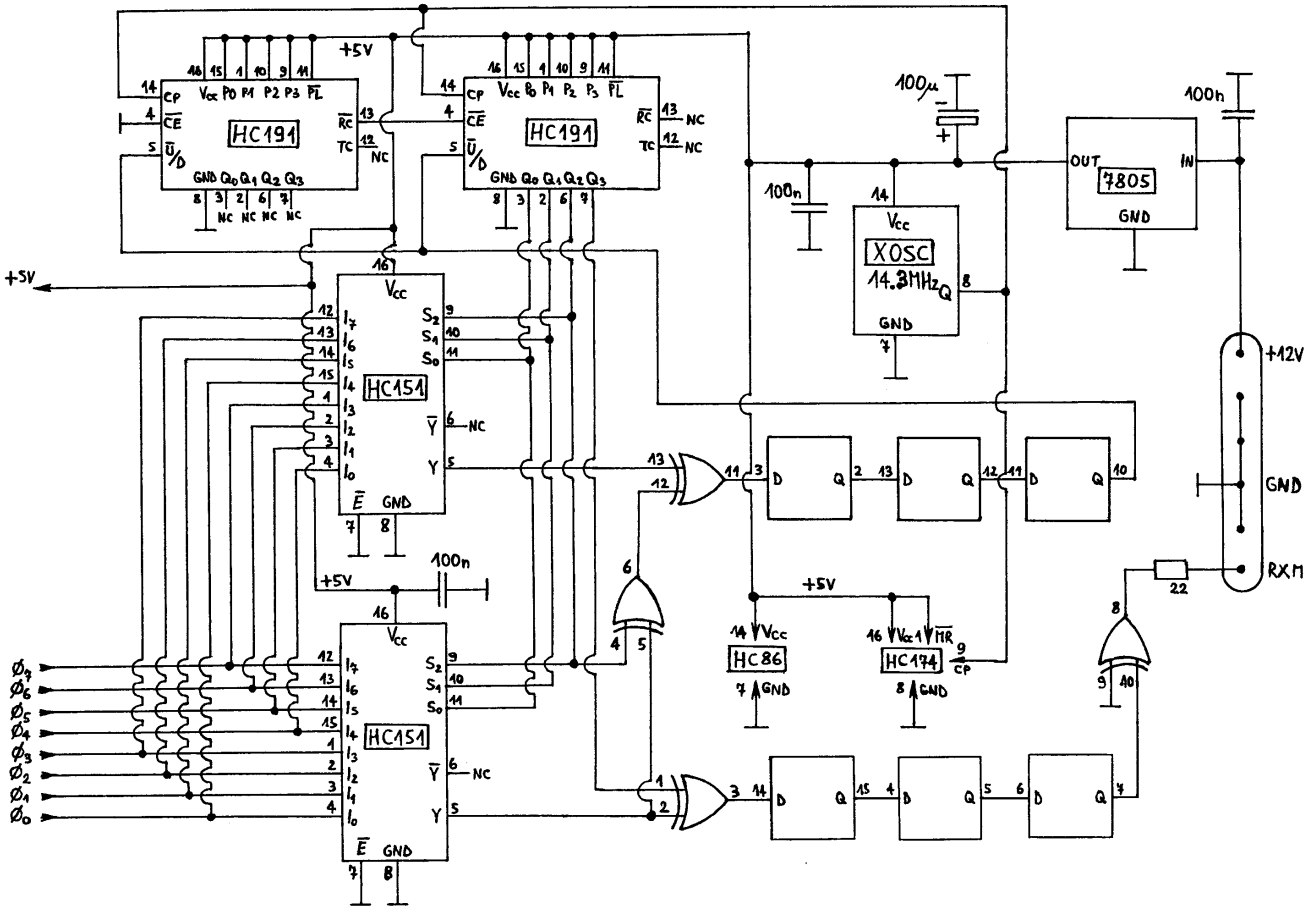


Figure 5 - Digital part of the demodulator: digital Costas loop.

The digital part of the new BPSK modulator is shown on figure 5. Two 74HC151 multiplexers are used as rotating switches, operated with an offset of 90 degrees. The output signal phase can be further flipped with EXOR gates (74HC86 pins 1,2,3 and 4,5,6) before the switching glitches are removed with the 74HC174 D-flip-flops. An EXOR gate (74HC86 pins 11,12,13) is also used to perform the signal multiplication, required for the feedback in a Costas loop.

The bidirectional counter is identical to the one used in the old BPSK demodulator and is built with two 74HC191 devices. The overall circuit was found to operate reliably up to clock frequencies of 20MHz. Since any switching glitches are completely removed by the D-flip-flops, the actual clock frequency can be increased from 6.144MHz to 14.3MHz, resulting in an increase of the carrier capture range from +/-24kHz up to about +/-56kHz.

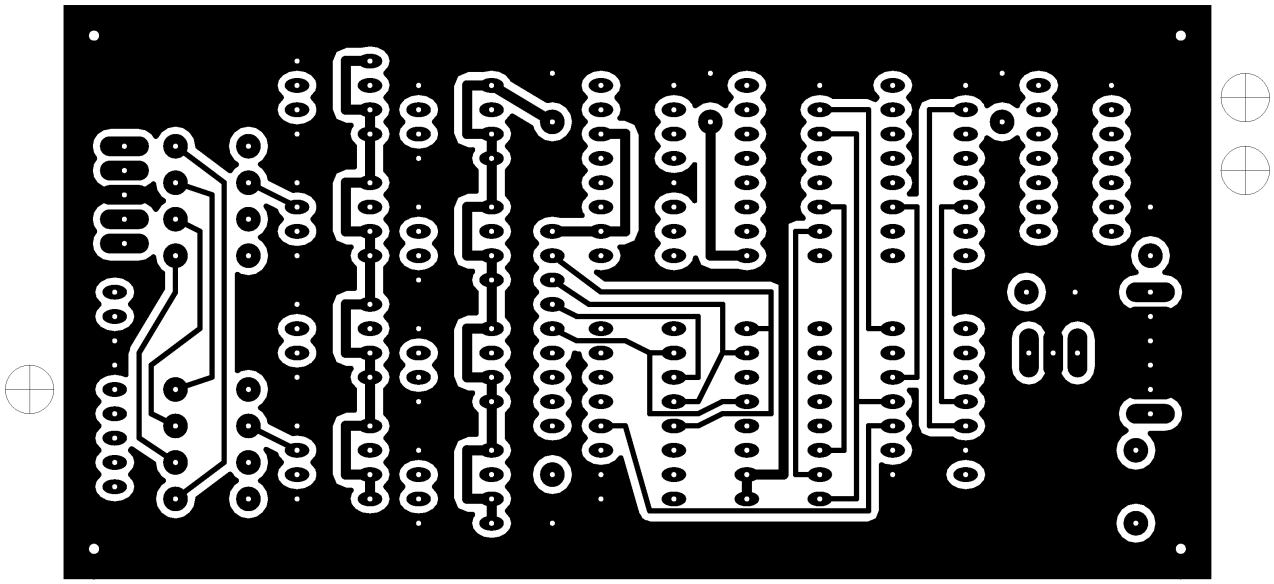


Figure 6 - Demodulator printed-circuit board, component side.

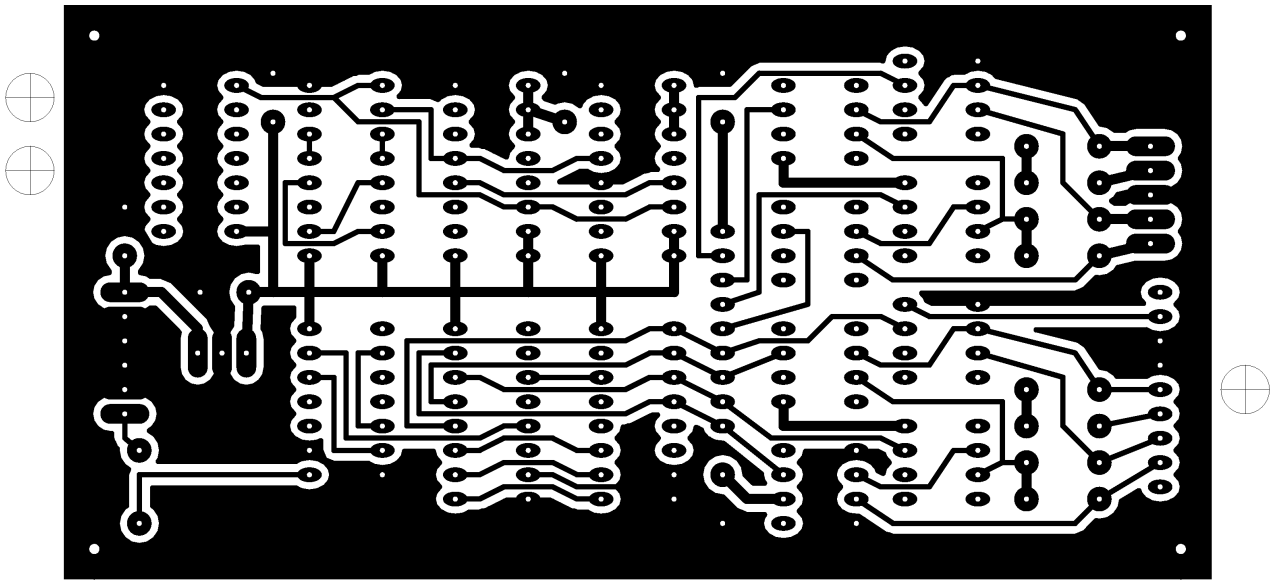


Figure 7 - Demodulator printed-circuit board, solder side.

The new BPSK demodulator is built on a double-sided printed-circuit board with the dimensions of 60mmX120mm. The component (top) side of the printed-circuit board is shown on figure 6 while the solder (bottom) side is shown on figure 7. The corresponding component location is shown on figure 8. The new BPSK demodulator has exactly the same dimensions and same electrical connections as the old one thus allowing a direct replacement of the old circuit.

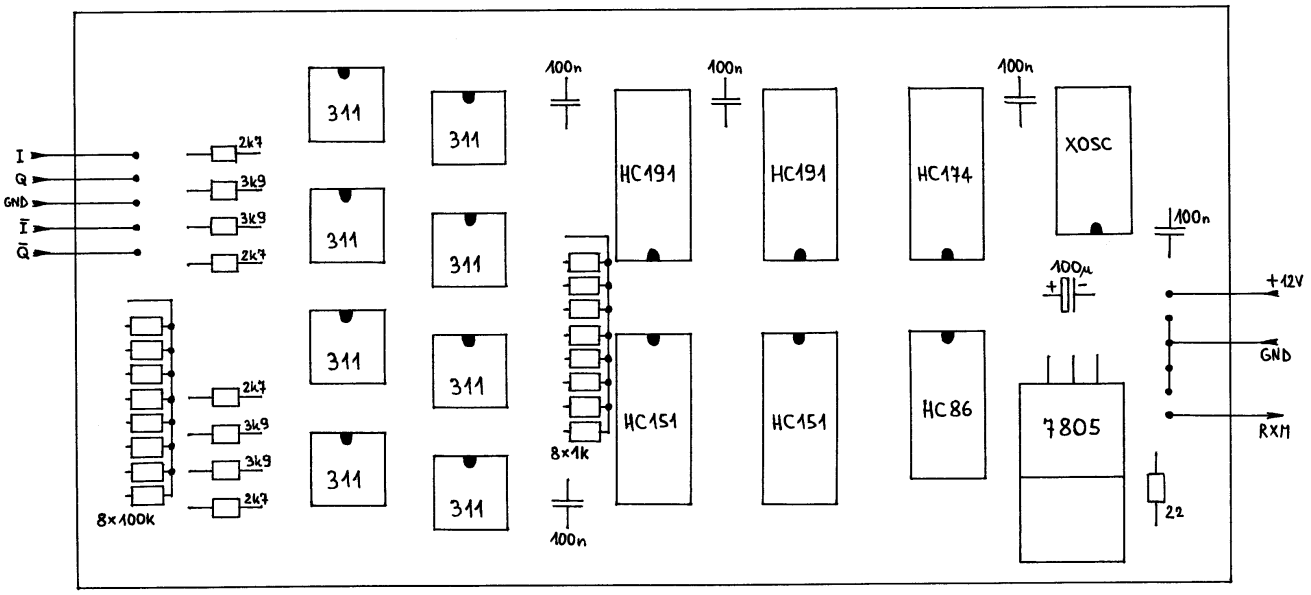


Figure 8 - Demodulator component location.

Besides removing switching transients, the new demodulator has a much improved input sensitivity and dynamic range. The new demodulator will operate without any performance degradation with the input signals in the range from 30mVpp up to 3Vpp, corresponding to a dynamic range of 40dB. On the other hand, the old BPSK demodulator with the 74HC4067 analog switches required signals between 1Vpp and 3Vpp, corresponding to a dynamic range of only 10dB.

3. Modification of the Zero-IF amplifier

The new BPSK demodulator on its own does not bring much improvement to the receiver performance, since most of the signal degradation occurs in the IQ dual IF amplifier. Thanks to its improved sensitivity and dynamic range, the new BPSK demodulator requires less gain in the IF strip and has much released AGC requirements. Of course, the IQ dual IF amplifier has to be modified or better completely rebuilt to make use of the improved demodulator.

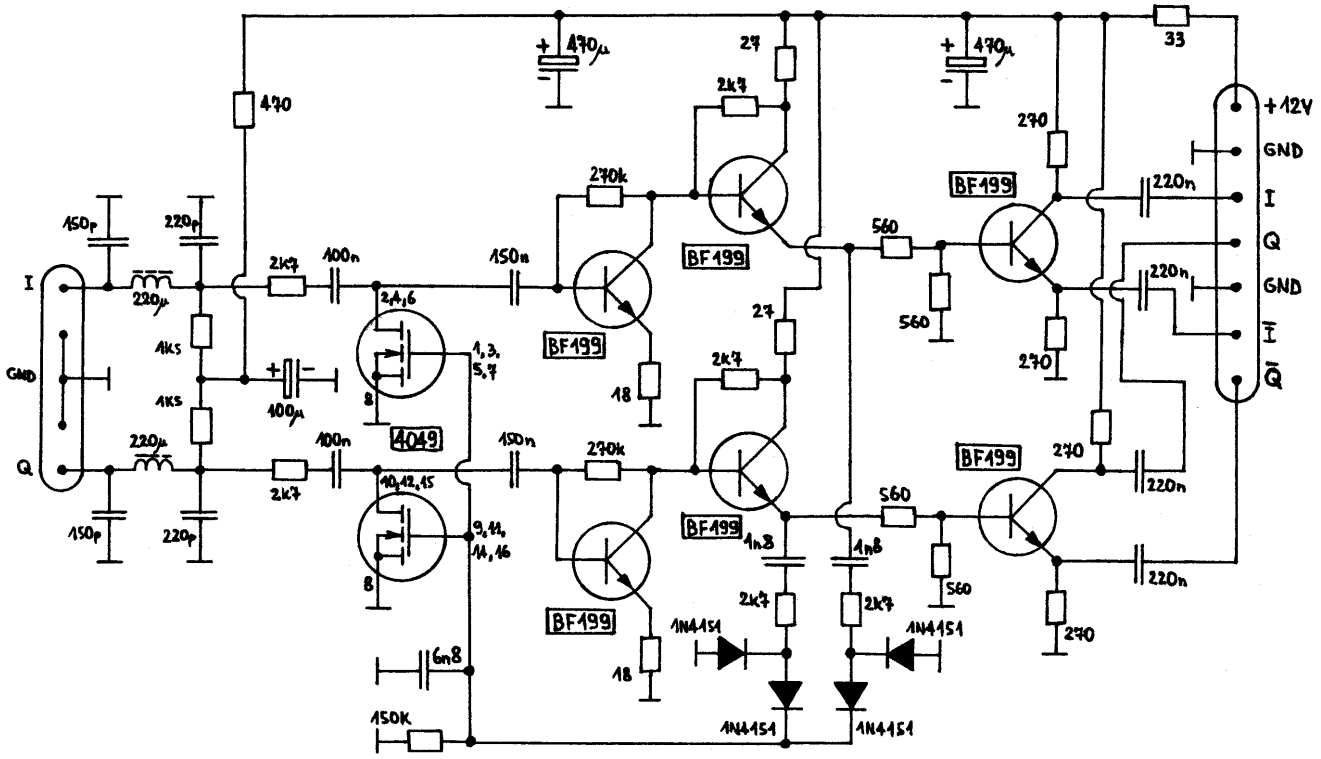


Figure 9 - Modified IQ dual IF amplifier.

The simplest solution is to modify the original IF amplifier as shown on figure 9. The original amplifier has three dual stages, while the new demodulator only requires a single dual IF amplifier stage with a common AGC. Thanks to the improved dynamic range of the demodulator, the AGC remains inactive at low signal levels thus minimizing the signal distortion.

The modified IQ dual IF amplifier can be built on the same printed-circuit board as presented in the original article [2], [4], [6] or [7]. Of course, only the components of first stage are installed, while the second and the third stage are simply bridged to the output symmetrical drivers. The values of some components are changed too. In particular the power-supply decoupling must be improved due to the lower signal levels required by the new BPSK demodulator.

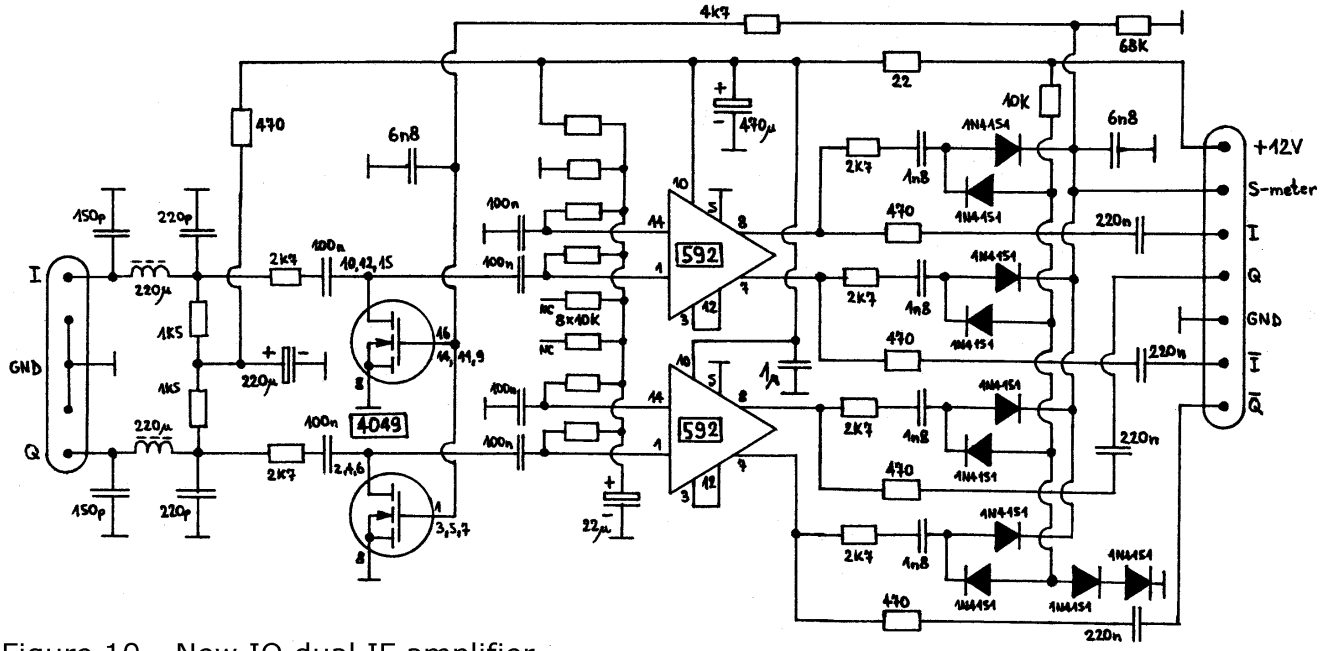


Figure 10 - New IQ dual IF amplifier.

A better solution is to redesign the IQ dual IF amplifier as shown on figure 10. The latter uses two NE592 (or two uA733) video amplifiers that already have symmetric outputs as required by the BPSK demodulator. The new IQ dual IF amplifier is equipped with a faster AGC detector. The AGC voltage is made available on the output connector to drive a high-impedance (>50kohm) S-meter. The latter is useful during transceiver checkout or troubleshooting.

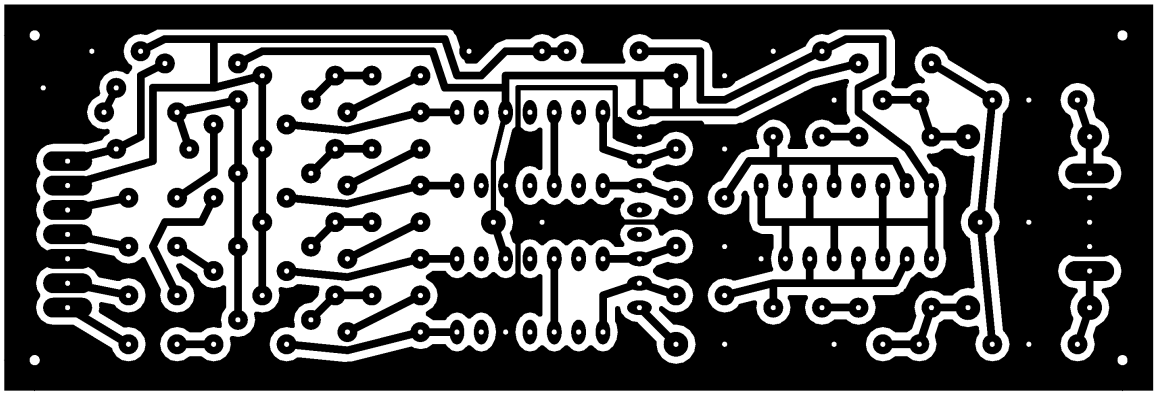


Figure 11 - New dual IF amplifier printed-circuit board.

The new IQ dual IF amplifier is built on a single-sided printed-circuit board with the dimensions of 40mmX120mm as shown on figure 11. The corresponding component location is shown on figure 12. The new printed-circuit board has the same length, but it is narrower than the old IF board. The electrical connectors are wired in the same way as in the old version, except for allocating an unused ground pin for the S-meter output.

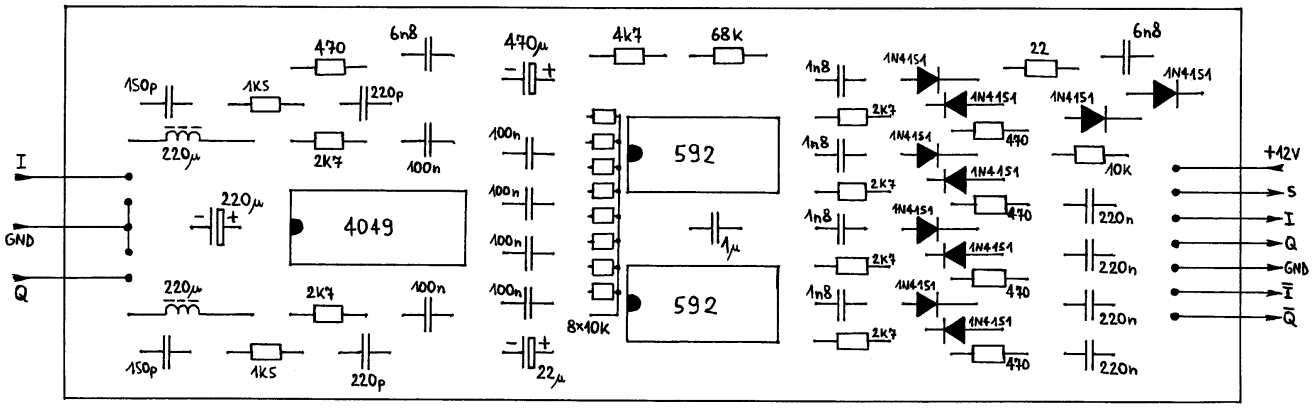


Figure 12 - New dual IF amplifier component location.

Finally, it is recommended to apply some small modifications also to the quadrature IQ mixer module of the receiver, in particular to the input coupling of both IF preamplifiers. For clarity, figure 13 shows the modification of one of the two IF preamplifiers. First, the two quarter-wavelength chokes L19 and L20 on the original circuit diagram should be replaced with 47uH chokes to improve the rejection of out-of-band signals. Second, the coupling capacitors should be decreased from 4.7uF down to just 1uF to speed-up the receiver recovery after an input overload.

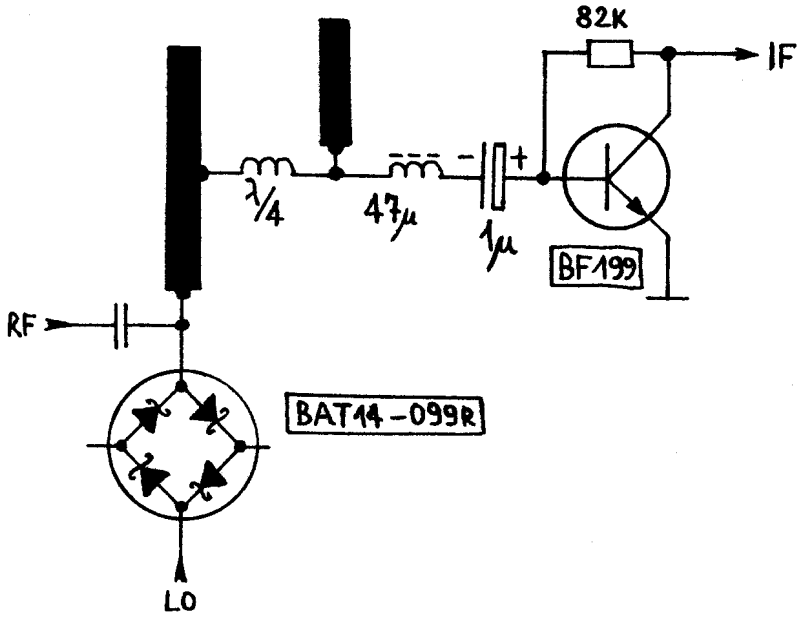


Figure 13 - Modification of the IF preamp.

4. Practical applications of the BPSK radios

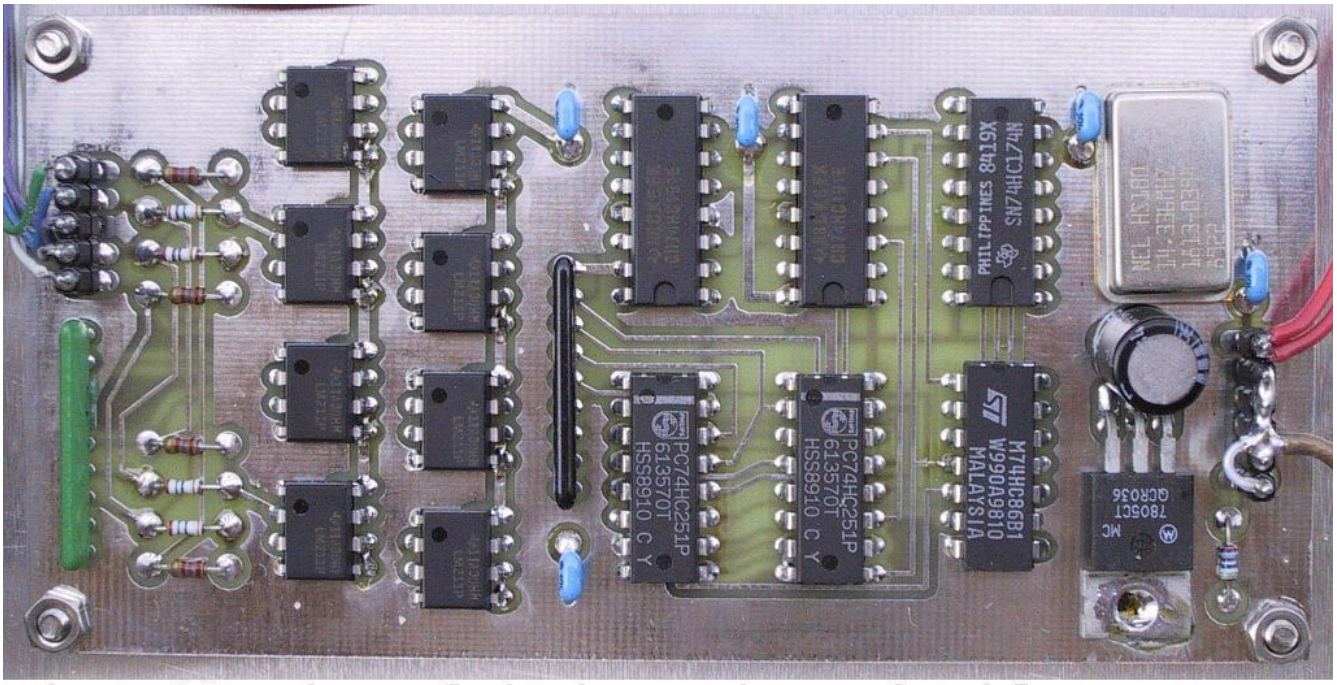


Figure 14 - Photo of the improved BPSK demodulator.

The described Zero-IF strip and BPSK demodulator represent a further improvement to the already successful BPSK megabit packet-radio transceiver. Besides the improved performance, the modules shown on figures 14 and 15 also feature a reduced circuit complexity and component count. Both modules were also tested successfully in a 13cm version of the Zero-IF BPSK transceiver to be published in a future article.

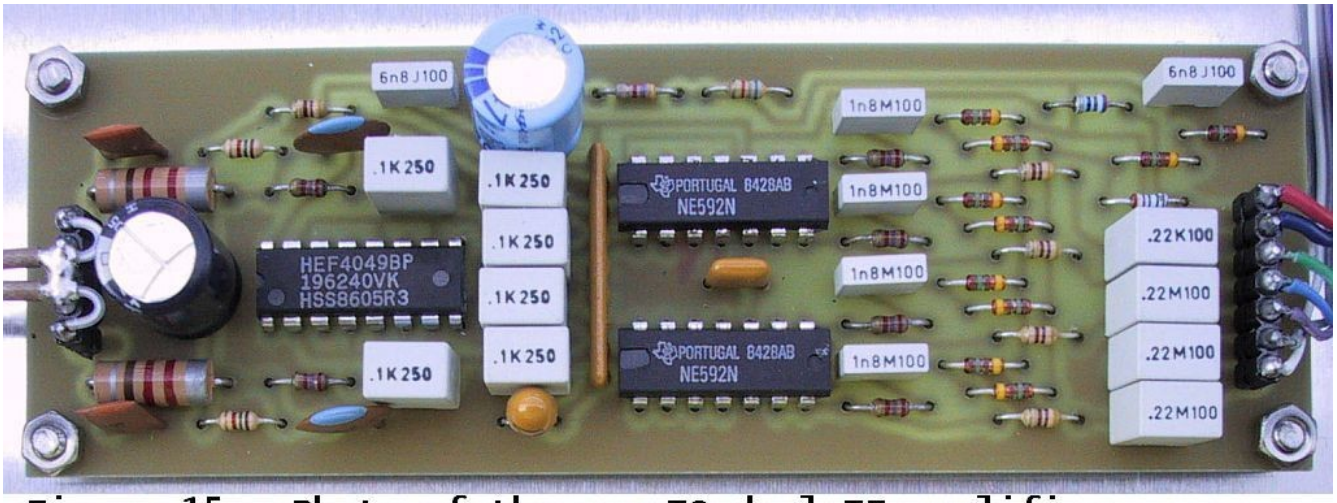
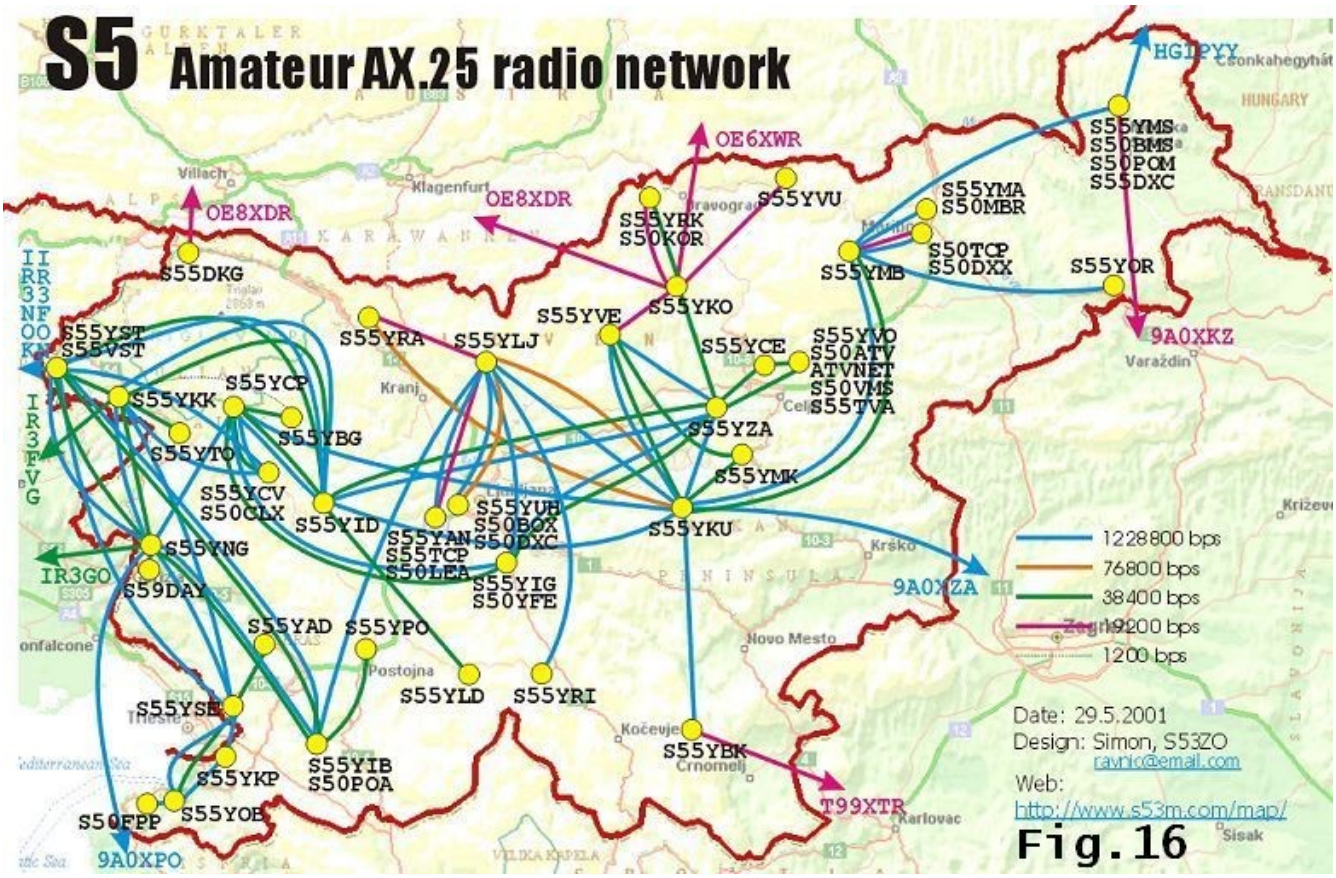


Figure 15 - Photo of the new IQ dual IF amplifier.

In order to increase the throughput of a packet-radio network, besides increasing the transmission speed it is also necessary to increase the frame length beyond the standard limit of 256 bytes. The current choice is 1500 bytes to transport standard IP frames without fragmentation and is already implemented in the megabit TNC shown in [8] or [9].

Longer frames are more sensitive to transmission errors. Therefore improving the demodulator performance is even more important with longer frames. If the (otherwise efficient) datagram mode is used to transmit IP frames through the AX.25 network, lost frames can only be recovered by the relatively slow TCP retries.



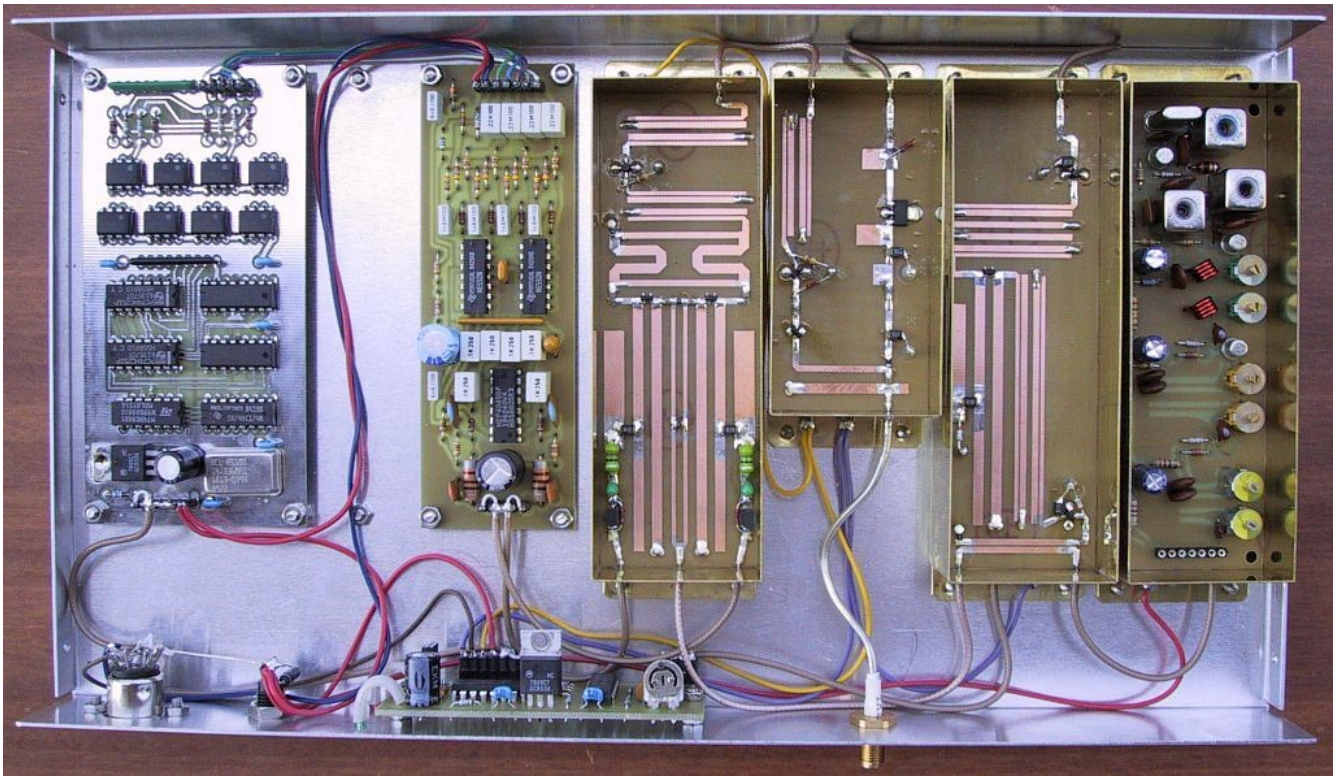
More than one hundred 1.2Mbit/s BPSK radios for both 23cm and 13cm have been built in Slovenia, Italy and Croatia. Practically the whole Slovenian packet radio network shown on figure 16 is now based on the Zero-IF BPSK transceivers, with many more nodes in Italy and Croatia adding to the list. While upgrading the network from 256byte frames to MTU 1500, some additional margin on the radio links was required and the latter was a good reason for developing an improved BPSK demodulator.

Since the megabit packet-radio network is available, digital ATV is becoming increasingly more popular, using inexpensive "web" cameras and personal computers. In order to obtain a good-quality, live color picture with programs like Microsoft Netmeeting, the RS-232 interface to the TNC has to be modified to at least 460kbit/s, resulting in data flows of about 30kbytes/s.

With these data flows, the current packet-radio network, based on 1.2Mbit/s radios, quickly approaches congestion. One already has to think about the next step, interlinks in the 10 to 20Mbit/s range. The described BPSK demodulator could in principle work at higher speeds by using faster comparators and faster logic. The best idea is probably to burn the whole digital circuit into a field-programmable logic array.

On the other hand, efficient and reliable BPSK demodulators are also required for satellite communications. Although the increased free-space insertion loss and tight power budget limit the data rate to less than 1Mbit/s for amateur satellites, simple and reliable hardware solutions are preferred to DSP, especially in a

radiation environment like space. The described BPSK demodulator can be easily modified for lower data rates, including the 153.6kbit/s BPSK "RUDAK" output from AO-40.



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[3] Matjaž Vidmar: "13cm PSK Transceiver for 1.2Mbit/s Packet Radio", 15th ARRL and TAPR DIGITAL COMMUNICATIONS CONFERENCE, Seattle, Washington, USA, September 20-22, 1996, pages 145-175.

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