# PLL-Based Fractional-N Frequency Synthesizers

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## Abstract

*Recent trends in the commercial use of fractional-N frequency synthesis can be attributed to the characteristic of independent loop bandwidth-channel spacing that results in low phase noise and relaxes the Phase-Locked Loop (PLL) design constraints. This paper reviews several techniques used to implement fractional-N frequency synthesizers and discusses the advantages and disadvantages. It also addresses design options and associated trade-offs.*

## 1. Introduction

Frequency synthesis is an inherent part of any communication system. As such communications systems are migrated into single integrated circuits or sets of integrated circuits, the inclusion of an optimal frequency synthesis technique as an integral part of the system-on-chip (SoC) is considered. Frequency synthesizers can typically be considered to be of two main varieties. The simplest tends to be the integer-N frequency synthesizer due to the fact that its output frequency is always an integer multiple of the reference frequency. The divider structure of the PLL-based frequency synthesizer or the edge-combiner topology of the DLL based frequency synthesizer provides insight on the simplicity of the integerr-N design. The PLL divider modulus is inherently an integer and similarly the DLL edge combiner forms the output waveform by operating over an integer number of reference cycles. Several implementation approaches for fractional-N PLL-based frequency synthesizers will be discussed in this paper.

## 2. PLL-based fractional-N frequency synthesizers

### 2.1. Background

The phase locked loop acts as a low-pass filter for reducing reference signal noise and low frequency path noise but appears as high-pass filter for VCO noise. As the VCO is the main contributor to the output phase noise, frequency synthesizer designers tend to use a wider loop bandwidth to suppress as much of the VCO noise as possible. However, for stability concerns and to suppress reference feed-through, the loop bandwidth must be approximately one order of magnitude smaller than the reference frequency. To have a higher loop bandwidth, a higher reference frequency must be used which in an integer-N frequency synthesizer translates to larger channel spacing. This direct trade-off between the loop bandwidth and the channel spacing in PLL-based integer-N frequency synthesizers is relaxed in fractional-N architectures by permitting the channel spacing to be equal to a fraction of reference frequency.

### 2.2. Advantages and drawbacks

In fractional-N frequency synthesizers the output frequency can be a fractional ratio of the reference frequency. It means the frequency resolution (channel spacing) is finer than the reference frequency. Given the same channel spacing, a fractional-N synthesizer can be designed with a higher loop bandwidth than an integer-N synthesizer. Higher loop bandwidth results in faster frequency switching and thereby dynamic bandwidth techniques can be used more efficiently [1,2]. In a dynamic bandwidth approach, the loop bandwidth is set to be wider than that desired when the PLL is outside of the lock-in-range to obtain a faster settling time during the transient mode. A higher reference frequency results in a higher comparison frequency that in turn relaxes the PLL requirements in terms of the noise reduction and the reference spur attenuation.

For a given channel spacing and a target output phase noise, the PLL noise requirement is smaller for the fractional-N architecture when compared to its integer-N counterpart due to the smaller divider modulus. The reference spur is also less sensitive to leakage current and non-ideal effects of the charge-pump [3].

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There are several approaches to designing fractional-N synthesizers but all are more complex as compared to the integer-N counterparts. Fractional-N synthesizers are inherently more spurious and may exhibit worse phase noise performance due to quantization issues. The wider loop bandwidth imposes more stringent requirements on in-band phase noise, and also increases the reference frequency, PD noise and the discrete spurious level.

### 2.3. Applications

Using a fractional-N architecture permits the realization of both phase and frequency modulations directly in the synthesizer and eliminates the need for up-conversion mixers in the transmitter thereby reducing the power consumption [4,5]. There is an emerging application in new radio systems such as TETRA, in which the channel spacing and the switching time specifications cannot be met with ordinary integer-N synthesizers. The high resolution of the fractional-N architecture can be used for automatic frequency control (AFC), Doppler correction or other such features that require tuning. This architecture can also used to relax the trade-offs in conventional integer-N synthesizers with the same loop bandwidth.

## 3. Fractional-N architectures

The challenge of designing a fractional-N frequency synthesizer involves a trade-off between phase noise, frequency switching speed, loop bandwidth, frequency resolution, tuning bandwidth and power consumption. The frequency multiplication factor is achieved by manipulating the divider modulus (which is inherently an integer) in a way that the average division ratio is the desired fractional ratio. This is implemented by using dividers with two or more division moduli and switching between the dividers. This switching strategy for the modulus dividers provides four fractional-N synthesizer techniques: pulse swallowing, phase interpolation, Wheatly random jittering and ΔΣ modulated jittering.

### 3.1. Pulse swallowing

A pulse swallowing fractional-N frequency synthesizer is shown in Fig. 1. It is similar to a conventional PLL-based integer-N frequency synthesizer with a dual modulus divider. The condition of overflow in the accumulator is used to shift the divider modulus from **n** to **n+1**. For a k-bit accumulator the average division factor N can be controlled by the accumulator input i as indicated in the following formula: $N = n + i/2^{k}$.

On every cycle of the divider output, i is added to the accumulator contents A, so the new accumulator value would be **A+i** unless the accumulator overflows, then the value assigned to accumulator is $A+i-2^{k}$. In the case of overflow, a carry output is generated that is used to switch the divider moduli. This is a simple approach that requires only one additional accumulator in hardware. A larger accumulator with a greater word length can provide a higher frequency resolution. The main drawback with this approach would be the spurious frequencies generated in the synthesizer output spectrum. These spurious tones result from the train of zeros and ones appearing on the carry output. As i aproaches zero or to $2^{k}$ equivalently, as the fractional ratio N approaches the integers n and n+1, this train of zeros and ones becomes longer and thus creates stronger spurious tones.

### 3.2. Phase interpolating

The phase interpolation approach uses a spur reduction technique to suppress the spurious tones as seen in the pulse swallowing approach. There are two types of spur reduction techniques used for this purpose: one compensates for the voltage error that causes the spur at the phase detector (PD) output and the other compensates for the phase error at the PD input. Fig. 2 shows amplitude compensation techniques applied to the PD output using a digital to analog converter (DAC). This approach is more effective with a sample and hold PD. For a sample and hold PD, the DAC must correct the PD output voltage to match its dc voltage for one reference clock period. The DAC uses the value of the accumulator that contains the information of the spurious beat tone to predict and compensate for the phase error. The drawback of this approach is the complexity of the DAC and sensitivity to process, supply voltage and temperature (PVT) variation.

Fig. 3 illustrates the phase compensation method [3]. Phase compensation is performed before the PD with the aid of a DLL. The settling time of the DLL should be much smaller than the PLL. The number of the stages, m, in the DLL provides the delay therefore the overall delay of each delay cell would be $T_{ref}/m$. If n is the smaller divider modulus, for n+i/m fractional values, the instantaneous phase error at the input of the PD can be corrected by sending the $i_{th}$ delay cell output

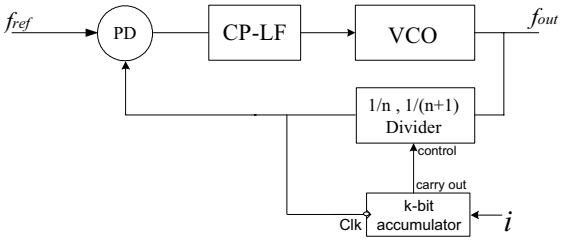


**Fig. 1. Pulse swallowing fractional-N synthesizer**

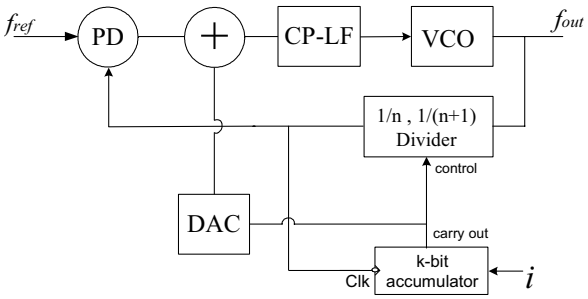


**Fig. 2. Amplitude compensation approach**

to the phase detector. As the result a phase correction equal to (1-i/m) X $T_{ref}$ is applied when the divider modulus changes to n+1. In this topology the DLL has to function at the frequency output of the synthesizer. The same phase compensation can be achieved by using a DLL with (m X k) delay cells and an input derived from a divide by k circuit. In this new configuration the DLL will work at a lower frequency but requires more delay cells. The main drawback of this approach is that the spurious tone can compensate completely for only n+i/m fractional values, and implementing a large value of m is not practical. This limits the resolution of this kind of synthesizer.

### 3.3. Random jittering

This spur reduction technique uses a random sequence generator to randomize the division modulus and thus converts the output spurs to jitter [6]. Fig. 4 shows a typical block diagram of such an implementation. A comparator is used to force the average of the divider moduli to the desired fractional ratio. The resolution depends on *k*, the number of bits of the random number generator and the comparator. The average divider moduli is controlled by *i*, the fix input of the comparator which is compared to random number generator output. The comparator output is one bit that controls the divider moduli. The main drawback of this approach is that the output spectrum exhibits a $1/f^2$ phase noise near the output frequency.

### 3.4. ΔΣ Modulated jittering

In this approach an over-sampling ΔΣ modulator is used to interpolate the fractional ratio with a coarse integer divider. Fig. 5 shows a typical fractional-N frequency synthesizer. The noise shaping ability of the ΔΣ modulator is used to shape the phase noise resulting from quantization and randomization to a higher offset frequency. This method can generate an arbitrarily fine frequency with digital modulation and when compared to the DAC method it is less sensitive to analog mismatch and PVT variations. It does however, have a relatively high complexity and power consumption.

## 4. ΔΣ fractional-N frequency synthesis

ΔΣ modulators were mainly used in over-sampling converters until Riley et al. [7] used the modulator noise shaping ability to improve the random jitter approach and to remove the $1/f^2$ phase noise. The natural high pass transfer function of a ΔΣ modulator pushes the close-in phase noise to high frequencies where the low-pass loop filter removes part of this high frequency noise. These synthesizers were recently used commercially [5,8,9] to provide small frequency step sizes, reduced output phase noise, reduced spurious tones and flexibility in the design.

### 4.1. Fundamental issues

The design of a ΔΣ fractional-N frequency synthesizer involves many trade-offs. The main trade-off is between in-band phase noise and quantization noise versus VCO noise, which includes noise coming from the power amplifier and circuit noise added in the loop filter. VCO noise can be suppressed by increasing the loop bandwidth. Decreasing the loop bandwidth can reduce both in-band phase noise and quantization noise. In-band phase noise has contributions from the reference signal path, the divider, the phase detector and the charge pump.

The optimum trade-off for each application is different. A QAM constellation with 1024 points requires very low in-band noise but for GSM and similar applications, which are sensitive to interference, the reduction of out-of-band phase noise is important.

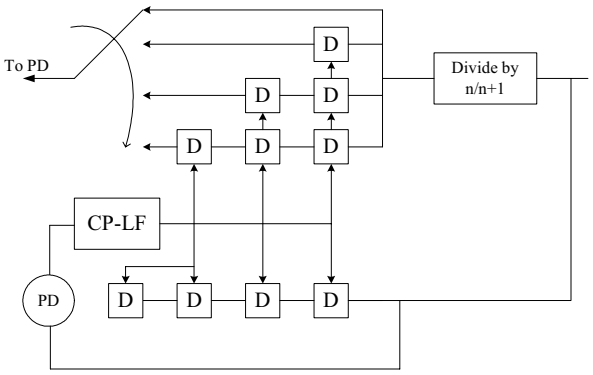


**Fig. 3. Phase compensation approach**

The source of in-band noise can be the jitter in digital logic, noise folding due to nonlinearity, charge- pump current noise, offset current noise and reference noise.

Digital logic jitter is a major contributor to in-band noise [10] and includes the contributions from the divider, the PD and the reference path. Non-linearities due to the PD dead-zone and the charge-pump modulate high frequency quantization noise into the signal bandwidth. This phenomenon is called noise folding and can be suppressed by controlling the distribution of the quantization noise and of the PD operating region [10].

### 4.2. ΔΣ modulators

In fractional-N synthesizers, the input of the ΔΣ modulator is usually a digital word representing the desired fractional value and the output of a ΔΣ modulator is a stream of integer numbers used to control the divider modulus. This stream forces the VCO output frequency to be a fractional ratio of the reference frequency. Over time, the average of the ΔΣ modulator output converges to the desired fractional ratio. All of the ΔΣ modulators involve to quantization noise but such noise is larger in single bit modulators.

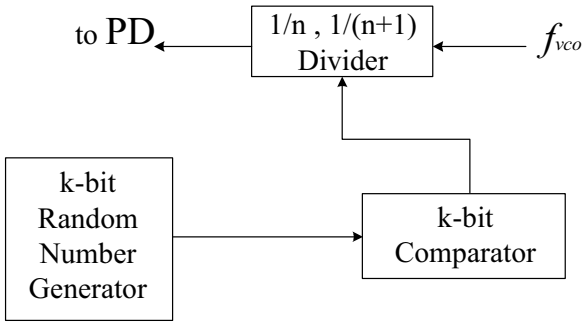


**Fig. 4. Random jittering approach**

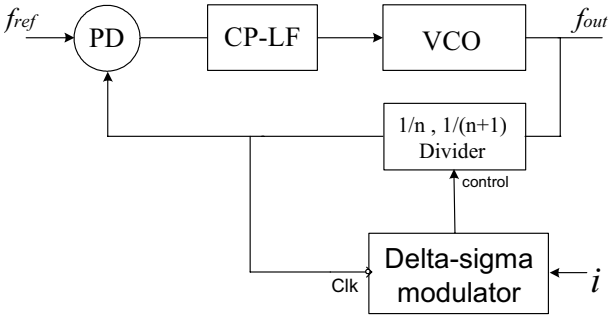


**Fig. 5. fractional-N synthesizer**

Multi-bit ΔΣ modulators may be used to reduce the quantization noise. The order of the ΔΣ modulator is equal to the number of integrators in the structure. Each integrator introduces a zero at the origin in its transfer function, and thus shapes the noise spectrum in the frequency domain. Converting the frequency to phase removes the zero from a first order ΔΣ modulator causing it to fail to randomize the quantization error and to thereby not remove spurious frequency components from the synthesizer output spectrum [7]. By selecting higher order ΔΣ modulators, the spurious energy is spread out and shaped to resemble high frequency noise, which is removed by the low-pass nature of the loop filter. The low frequency components of quantization nonlinearity error are filtered more by the higher order ΔΣ modulator. The output noise spectral density of the higher order modulators increases at greater rates per unit frequency resulting in a greater SNP in the base-band at the cost of increased out-of-band noise. When higher order modulators are used, the PLL requires extra poles in the loop filter to suppress the quantization noise at a high frequency. In practice both in-band and out-of-band noise affects the synthesizer performance but the high frequency noise is difficult to suppress with a finite number of PLL poles [8]. Second and third order ΔΣ modulators are used in practice for fractional-N synthesizers [4][5][7][8][16].

### 4.3. Modulator architectures

The choice of the appropriate ΔΣ modulator structure for fractional-N synthesis requires the consideration of many factors including noise shaping, spurious content of the output spectrum, output levels, loop filter order and circuit complexity. Both analog and digital implementation of these architectures is possible but the digital implementation is more common in fractional-N synthesizers. In a digital implementation, an accumulator acts as an integrator and a comparator. As it also has a feedback path, the

accumulator can be considered as a compact first order ΔΣ modulator [16]. Digital ΔΣ modulators do not have non-idealities and overload is not a problem as long as they are stable. Cascade digital modulators do not suffer from mismatch or noise leakage from the input stage (unlike the analog counterparts) and multi-bit quantizers do not suffer from non-linear effects. High order modulators can be realized with interpolative and MASH (Multi-stage noise shaping) architectures.

MASH architectures use a cascade of lower-order structures to construct a high-order modulator [17]. It usually constructed by cascading first order modulators or a combination of first and second order modulators. A MASH modulator produces a multi-bit output, which must control a multi-modulus divider. In general a multi-bit modulator can achieve more desirable noise shaping for frequency synthesis. A programmable counter can serve as multi-modulus divider but such a counter can be hard to implement for very high speeds. An estimate for the hardware complexity of a MASH modulator can be found in [18]. MASH offers a simpler high order architecture with no stability problems and tends to generate widespread high frequency bit patterns that imposes more stringent requirements on PD design.

Compare to single-loop modulators, the intensive switching of the MASH ΔΣ modulator increases the high frequency noise and causes larger instantaneous phase error. A fourth-order MASH provides a higher order of noise shaping (-80 dB/dec) but it has almost twice the complexity of the third-order MASH and consumes more power. As it shown in Fig. 6 and Fig. 7 , third-order MASH can realized from a MASH 1-1-1 and MASH 1-2, which are a cascade of three first order modulators or a cascade of one first-order and one second-order [19] modulator, respectively. MASH 1-1-1 and MASH 1-2 exhibits the same order of noise shaping however the MASH 1-2 can be designed to have four output levels instead of eight for the MASH 1-1-1 [18]. A disadvantage of the MASH 1-2 is that it only allows the input to operate at about 75% of the whole fractional range [18].

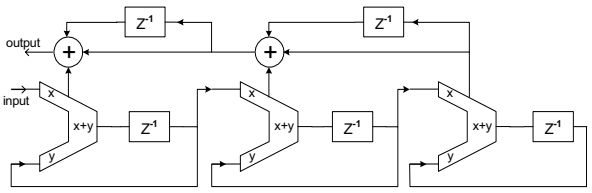


**Fig. 6.**

Single-loop (also called interpolating or single-stage) ΔΣ modulators introduce less phase noise and

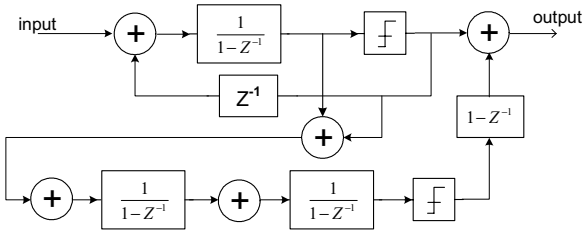


**Fig. 7. The block diagram of MASH 2-1 modulator**

can provide either a single-bit or a multi-bit output. However it is subject to instability and a smaller input range. The latter can be eliminated with a multi-bit quantizer in a digital implementation. A typical third-order single-loop multiple-feedforward ΔΣ modulator is shown in Fig. 8. The quantizer output is limited to three levels and the feedforward branches can be truncated to reduce the complexity. Another version of the single-loop which uses multiple-feedback [20] is shown in Fig. 9. In order to obtain a reasonably stable input range, a large number of quantization levels is required (i.e. nine here). The bit-length of the adders before the accumulators are much shorter than the accumulators themselves [21]. A tone free output can be achieved at the cost of high output levels.

Table I shows a performance comparison of third-order ΔΣ modulators. The wide-spread output pattern of a MASH modulator makes the synthesizer more sensitive to the substrate noise coupling since the turn-on time of the charge-pump in the locked condition increases. This can reduce by limiting the output range of the modulator [8]. The smaller on-time of the CP in a single-loop modulator, makes it less sensitive to noise coupling from substrate and power supply. Due to non-linear mixing in PD and CP, noise at *fref/2* folds back to a lower frequency similar to multi-bit ΔΣ ADCs. For a single-loop modulator, noise at *fref/2* is much lower and thus its noise leakage due to non-linearity is also lower. Although the ideal in-band phase noise is lower for the MASH ΔΣ modulator, due

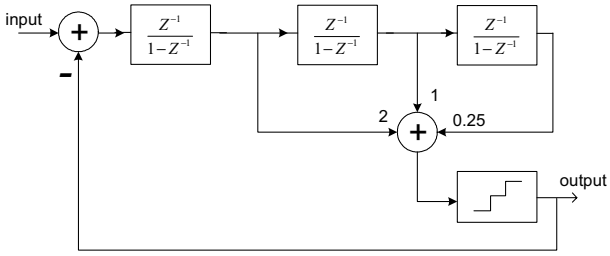


**Fig. 8. Single-stage 3rd-order feedforward architecture**

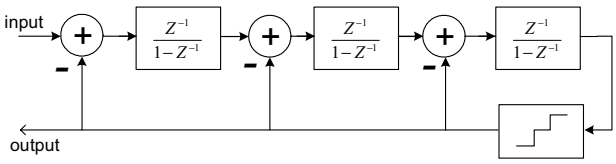


**Fig. 9. Single-stage 3rd-order feedback architecture**

to higher phase error introduced by this modulator, only a small non-linearity is enough to increase the in-band noise more than expected from a single loop modulator. The single-bit high-order modulators have a dead-band problem due to the limited input range of the quantizer in synthesizer applications. The non-ideal effects at the band edges can be reduced by extending the input range with a multi-level quantizer [8].

## 5. Implementation considerations

The division modulus is modulated by the ΔΣ output, by the desired mean value as well as by the shaped high frequency quantization noise. A main advantage of the fractional-N synthesizer is the decoupling of the choice of the reference frequency and the PLL bandwidth. To ensure that the modulator does not corrupt the rms phase error, the dynamic range of the modulator must be higher than that of the frequency synthesizer [8].

The dynamic range of a frequency synthesizer is defined as the ratio of the largest possible frequency change to the smallest one. The largest frequency change is the full frequency range of the modulator within the modulus range. In a fractional-N synthesis application, the ΔΣ input is a constant number, and thus the output sequence may not be long enough to be of practical use. The periodic nature of a short sequence can cause spurious tones in the synthesizer output. A simple way to achieve a longer output sequence is to increase the bit-length of the input but this also increases modulator complexity and the power consumption.

To reduce the fractional spurs resulting from a limited output sequence, some perturbation is imposed in ΔΣ output sequence by applying a dithering signal from a pseudo-random generator to the input. In [18] the carry-in input of the adder is used in a feedback path to randomize the input. In [25], a 14 dB suppression of spurious tones is achieved by using the 3 output bits of the MASH modulator as a dithering signal to replace the least significant bits of the modulator.

## 6. Simulation issues

The high output frequency of the synthesizer imposes the use of a high simulation sample frequency. However, the overall dynamics of the loop have typically a much lower bandwidth. The fractional-N synthesizer exhibits a non- periodic behavior in steady state, which prevents the use of methods developed for periodic steady-state conditions [11]. In [12] an area conservation principle is used to convert a continuous time phase-frequency detector (PFD) output to a discrete time sequence and to thus use a uniform step size for simulation. In the next step the VCO and the divider as assumed to be used as one block that allows a much smaller sampling period in the simulation [12].

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## 8. Multi-phase fractional-N synthesizer

Although a multi-modulus divider can achieve an arbitrary fractional ratio, the minimum phase jump at the divider output is still equivalent to one VCO period

**Table 1. Performance comparison of 3rd-order modulator [22]**

| Architecture | MASH 1-1-1 | MASH 2-1 | Single-stage feedforward | Single-stage feedback |
|---|---|---|---|---|
| Noise shaping | good | fair | fair | good |
| Spurious tones | very | some | a few | free |
| Output levels | 8 (-3 ~ 4) | 4 (-1 ~ 2) | 3 (0 ~ 2) | 9 (-4 ~ 4) |
| Working clock | fout | 0.5 fout | almost fout | 0.33 fout |
| Stable dc input range | 0 ~ 1 | 0.125 ~ 0.875 | 0.263 ~ 1.678 | -2.5 ~ 2.5 |

In [13,14] a finer resolution is achieved by interpolating the phases using multi-phase VCOs having a phase jump smaller than one VCO period at the divider output. However, the phase mismatch (i.e. the phase inaccuracy of the multi-phase VCO outputs) gives rise to fixed spurs when the output phases are selected sequentially. In [15] modulation is used in combination with phase interpolation to eliminate the spurs. A smaller phase jump at the divider output decreases the equivalent quantization step size and consequently the equivalent quantization noise of the modulator. This approach shows lower phase noise than in the multi-modulus approach. A block diagram of a multi-phase fractional-N synthesizer is shown in Fig. 10.

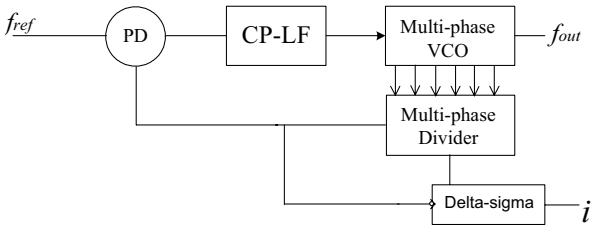


**Fig. 10. Multi-phase fractional-N synthesizer**

## 9. Conclusion

This paper provides an overview of PLL-based fractional-N frequency synthesis. A discussion is provided on structures of PLL-based implementations found in available literature outlining the merits of each technique, the implementations and simulation issues.

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