 By Ken Holladay, Fujitsu Microelectronics

USING A SIMPLE PROCEDURE AND SET OF EQUATIONS, YOU CAN EASILY DESIGN A FREQUENCY SYNTHESIZER TO MEET SPECIFICATIONS BASED ON THE LOOP BANDWIDTH INSTEAD OF THE HOP TIME. HOP TIME DEPENDS ON THE LOOP BANDWIDTH, SO YOU MAY HAVE TO MAKE COMPROMISES IN THESE TWO SPECIFICATIONS TO MEET DESIGN REQUIREMENTS.

Design a PLL for a specific loop bandwidth

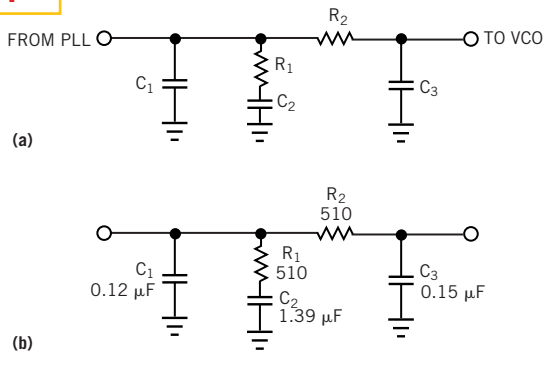
Today's PLL ICs make designing a high-quality, versatile frequency synthesizer easier than ever. These devices have many built-in functions, such as serial interfaces, phase detectors, and swallow counters. Typically, the only external parts are the reference oscillator, VCO, loop filter, and dc decoupling components. Some ICs, such as the MB-15E03SL from Fujitsu (www.fujitsumicro.com), also have built-in circuitry for a crystal or an LC reference oscillator. Most of the synthesizer applications are for wireless designs, for which the system specifications require the synthesizer to operate over a bandwidth of 10% or less.

Most of the written design information about calculating the loop filter for these PLL synthesizers is based on how long it takes to "hop" from one frequency to another. This design information is sufficient if you plan to use the synthesizer only as a local oscillator, to convert one frequency to another, or as a continuous-wave source at various frequencies. However, many applications use a synthesizer to modulate a transmitter. In this case, the loop bandwidth may be the controlling factor for the loop-filter design.

You can apply modulation to a synthesizer by changing the VCO tuning voltage either before or after the loop filter. The frequency response of the modulation at the output of the transmitter will have either a lowpass or highpass characteristic, depending on where in the loop you apply the modulating signal. The PLL's loop bandwidth sets the corner frequency of this response. There are some systems that insert the modulation both before and after the loop filter to get a flat response.

If you plan to phase- or frequency-modulate the PLL, the desired loop bandwidth will influence the choice of the loop-filter component values. Therefore, you must base the initial design on the desired loop bandwidth. Unfortunately, trade-offs are necessary. A direct relationship exists between loop bandwidth and hop time: The narrower the bandwidth, the longer it takes the synthesizer to step from

Figure 1



For the typical loop-filter configuration (a), you can use a design method based on loop bandwidth to arrive at standard component values (b).

one frequency to another. If hop time is also important, you have to work out a balance between loop bandwidth and hop time.

DEFINE THE BASIC REQUIREMENTS

To design a loop filter based on bandwidth, instead of the frequency hop or switching time, consider the following example. You first define the basic synthesizer requirements:

- Frequency range: 770.01 to 800.01 MHz;
- Channel spacing: 30 kHz;
- Maximum frequency hop: 30 MHz; and
- Loop bandwidth: 1000 Hz.

Then, you identify the active component specifications:

- VCO sensitivity: 22 MHz/V and
- PLL IC charge-pump current: 6 mA.

Now, you perform the PLL calculations for the typical loop-filter configuration in **Figure 1a**. **Table 1** lists the definitions of terms. The basic steps and calculations for a given loop bandwidth are as follows:

1. Calculate F_{STEP}:

F_{STEP} = MAXIMUM VCO FREQUENCY −MINIMUM VCO FREQUENCY.

2. Calculate N:

$$N = \frac{\text{MAXIMUM VCO FREQUENCY}}{\text{CHANNEL SPACING}}.$$

3. Calculate F_N:

$$F_N = \frac{2 \times \text{LOOP BANDWIDTH}}{2\pi \times \left(\xi + \frac{1}{4 \times \xi}\right)}.$$

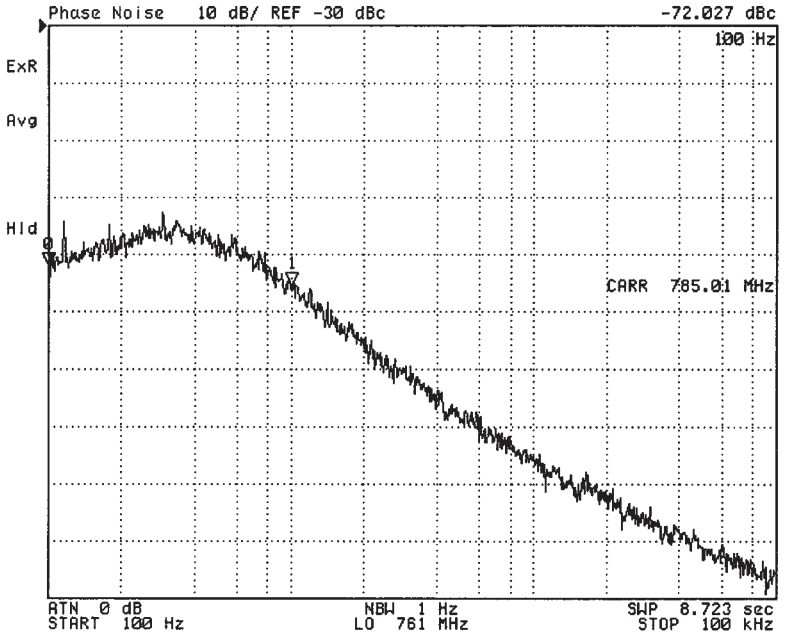


Figure 2 The phase noise at 100 Hz (marker 0) is −72.0 dBc/Hz, and the phase noise at 1000 Hz (marker 1) is −75.5 dBc/Hz.

4. Calculate C_2:

$$C_2 = \frac{I_{CP} \times K_{VCO}}{N \times (2\pi \times F_N)^2}.$$

5. Calculate R_1:

$$R_1 = 2 \times \xi \times \sqrt{\frac{N}{I_{CP} \times K_{VCO} \times C_2}}.$$

6. Calculate C_1:

$$C_1 = \frac{C_2}{10}.$$

7. Choose values of R_2 and C_3:

R_2 and C_3 reduce any spurs that the reference frequency introduces. The product of R_2 and C_3 should be at least one-tenth times the product of C_2 and R_1.

8. Calculate T_S:

$$T_S = \frac{-1 \times \left(\ln \frac{F_A}{F_{STEP}}\right)}{F_N \times 2\pi \times 2\xi}.$$

TABLE 1–DEFINITION OF TERMS

Term	Description
F_A	The frequency of the carrier within the desired time (T_S) after a step or hop; normally, 1000 Hz
F_N	Natural frequency
F_{STEP}	Maximum frequency change during a step, or hop, from one frequency to another
I_{CP}	Charge-pump current
K_{VCO}	VCO sensitivity
T_S	The desired time for the carrier to step to a new frequency
ξ	Damping factor; typically, 0.707

STEP-BY-STEP EXAMPLE

(1) F_{STEP} = 800.01 MHz − 770.01 MHz = 30 MHz.

(2) $$N = \frac{800.01e^6}{30e^3} = 26{,}667.$$

(3) $$F_N = \frac{2 \times 1000}{6.28 \times \left(0.707 + \frac{1}{2.828}\right)} =$$ 300.27 Hz.

(4) $$C_2 = \frac{0.006 \times 22e^6}{26{,}667 \times (6.28 \times 300.27)^2}$$ = 1.39 µF.

TABLE 2–HOP TIMES FOR VARIOUS LOOP BANDWIDTHS

Loop bandwidth (Hz)	Hop time (msec)
500	15.5
1000	7.7 (design example)
2000	3.9
3000	2.6

$$R_1 = 2 \times 0.707 \times \sqrt{\frac{26{,}667}{0.006 \times 22e^{6} \times 1.39e^{-6}}} = 539\Omega. \quad (5)$$

$$C_1 = \frac{1.39\,\mu F}{10} = 0.139\,\mu F. \quad (6)$$

7. Let R_2=539Ω. Then, C_3=1.39 µF/10=0.139 µF.

$$T_S = \frac{-1 \times \left(\ln \frac{1000}{30e^{6}}\right)}{300.27 \times 6.28 \times 0.707} = 7.73\ \text{msec}. \quad (8)$$

Figure 1b shows the completed design using the closest standard component values. The measured results of this design working with an MB15E03SL-based synthesizer show a close relationship between the design goals and the actual performance. **Figure 2** displays the phase noise between 100 Hz and 100 kHz. The phase noise at 100 Hz (marker 0) is −72.0 dBc/Hz, and the phase noise at 1000 Hz (marker 1) is −75.5 dBc/Hz. **Figure 2** also shows that the loop bandwidth is very close to the desired 1000 Hz.

Figure 3 shows that the spurs are greater than −96.7 dBc at 30 kHz from the carrier. **Figure 4** shows that the hop time from 770.01 to 800.01 MHz is 7.65 msec. The loop bandwidth mainly determines this hop time. **Table 2** shows the approximate hop times that result when you use other loop bandwidths in the design example.□

AUTHOR'S BIOGRAPHY

Ken Holladay is applications manager for the wireless group at Fujitsu Microelectronics. He has been with FMI for five years and has more than 20 years of industry experience.

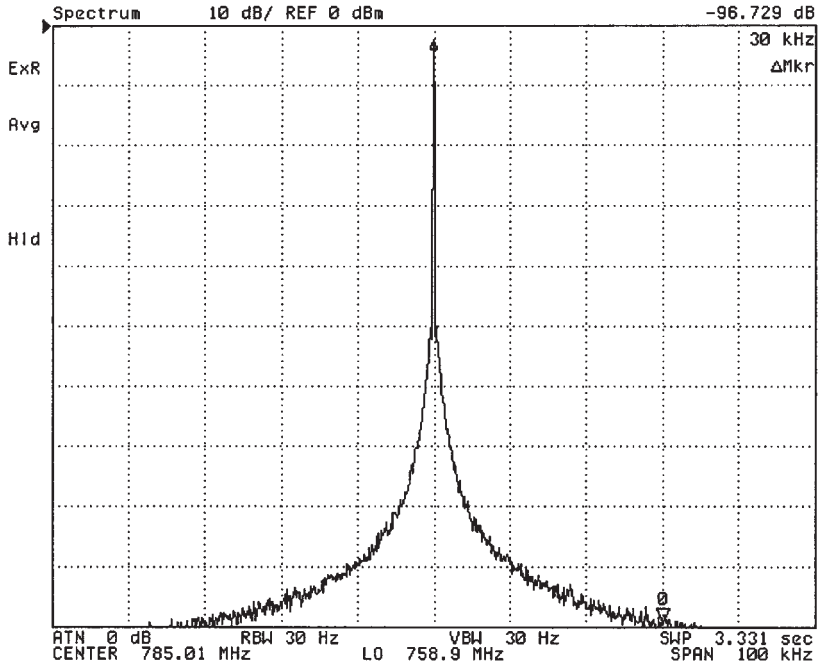


Figure 3 The spurs are greater than −96.7 dBc at 30 kHz from the carrier.

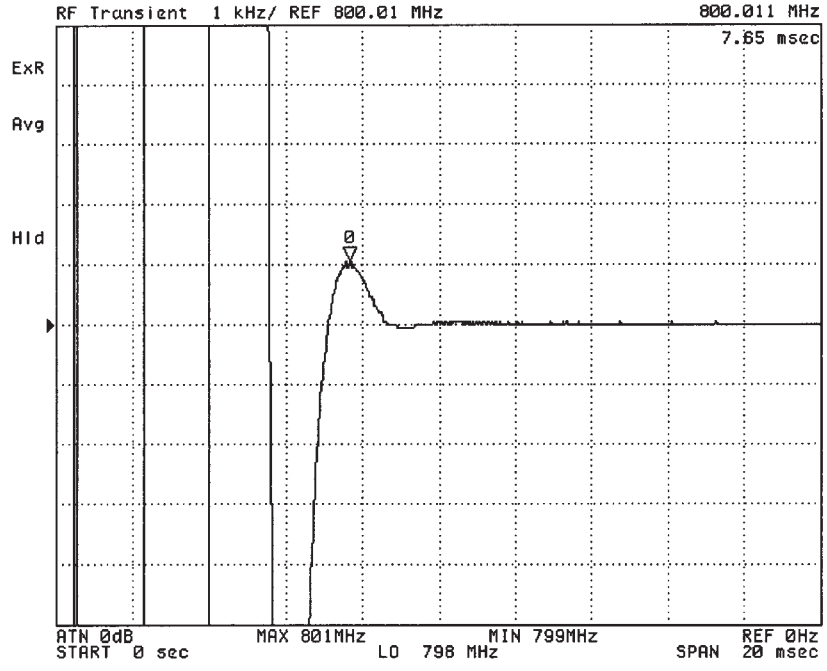


Figure 4 The hop time from 770.01 to 800.01 MHz is 7.65 msec.