# BK4815N Application Note

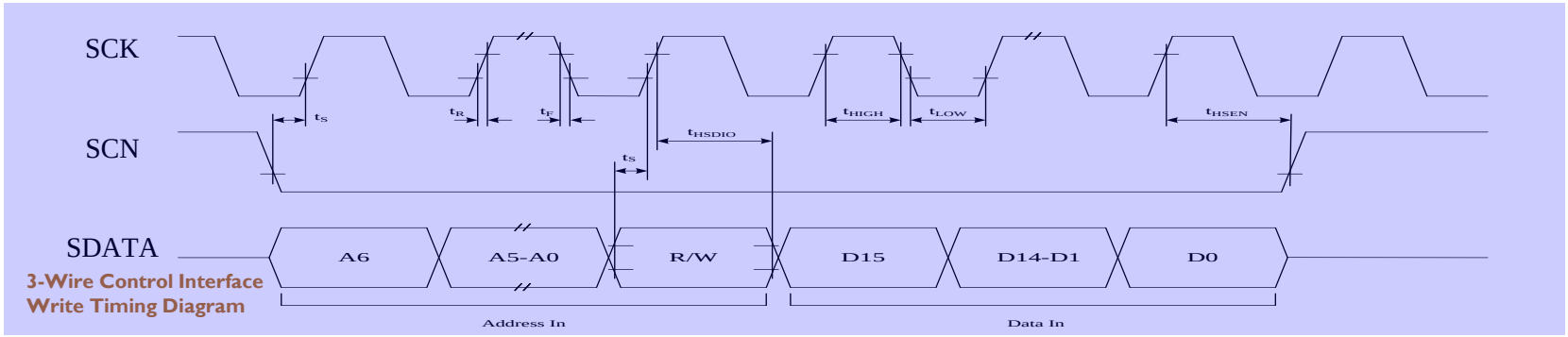
V1.0

# Index

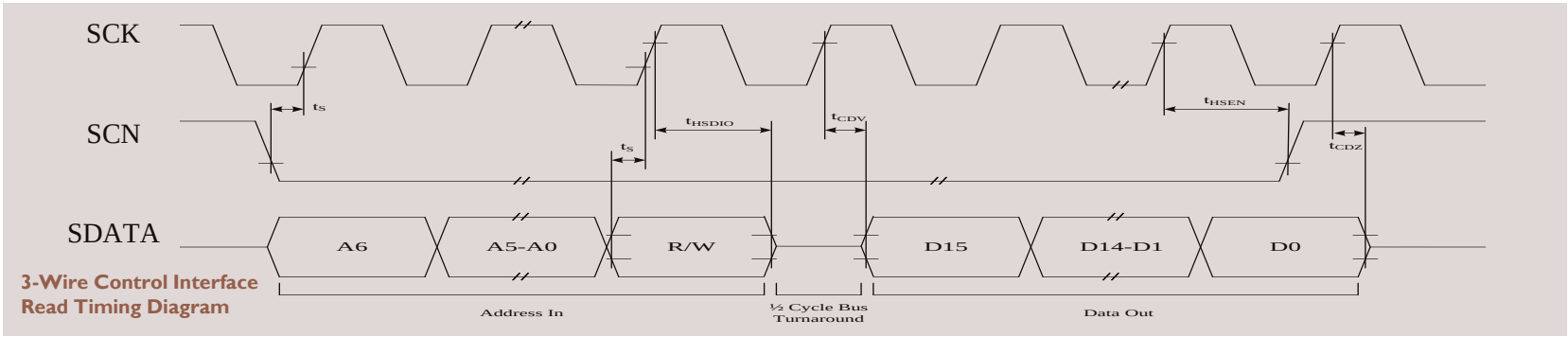

- MCU Interface
- Register Initialization
- TX Audio
- RX Audio
- AFC
- CTCSS
- CDCSS
- SELCALL
- DTMF
- FSK
- VoX
- Squelch
- Power Saving
- TX/RX Mode Switch
- Pop Sound
- SINAD, RSSI, Ex-Noise
- Frequency Settings
- VCO Coverage
- VCO Calibration
- TX Ramping
- TX Output Power
- Image Interference Rejection
- RX AGC
- Interrupt
- GPIO
- Loop Back Mode
- Channel Spacing
- Digital Walkie-Talkie
- Hardware Design

# MCU Interface – 3 Wire SPI

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCK Frequency | $f_{CLK}$ | | 0 | — | 8 | MHz |
| SCK High Time | $t_{HIGH}$ | | 25 | — | — | ns |
| SCK Low Time | $t_{LOW}$ | | 25 | — | — | ns |
| SDATA Input, SCN to SCK ↑ Setup | $t_S$ | | 20 | — | — | ns |
| SDATA Input to SCK ↑ Hold | $t_{HSDATA}$ | | 10 | — | — | ns |
| SCN Input to SCK ↓ Hold | $t_{HSCN}$ | | 10 | — | — | ns |
| SCK ↑ to SDATA Output Valid | $t_{CDV}$ | Read | 2 | — | 25 | ns |
| SCK ↑ to SDATA Output High Z | $t_{CDZ}$ | Read | 2 | — | 25 | ns |
| SCK, SCN, SDATA, Rise/Fall Time | $t_R$ , $t_F$ | | — | — | 10 | ns |




3-Wire Control Interface
Write Timing Diagram




3-Wire Control Interface
Read Timing Diagram

# Register Initialization

- All analog registers(REG02~REG16, REG107~REG109) should be set to the target value after power on.
- For digital registers(REG01, REG17~REG106, REG112~REG127), there is a built-in value after power on. Therefore, for each register, if its target value is according with the built-in value, you don't have to write the target value into this register.

| REG (DEC) | Built-in Value | REG (DEC) | Built-in Value | REG (DEC) | Built-in Value | REG (DEC) | Built-in Value | REG (DEC) | Built-in Value |
|---|---|---|---|---|---|---|---|---|---|
| 01 | 0x0000 | 40 | 0x0A20 | 59 | 0x2206 | 81 | 0xB200 | 101 | Read Only |
| 17 | 0x8800 | 41 | 0x0FFF | 60 | 0x721B | 82 | 0x0000 | 102 | 0x0000 |
| 18 | 0x4064 | 42 | 0x0000 | 61 | 0xC235 | 83 | 0x0000 | 103 | 0xB1A2 |
| 19 | 0x3FFF | 43 | 0x4000 | 62 | 0x1100 | 84 | 0xFC46 | 104 | 0x143C |
| 20 | 0x0000 | 44 | 0x683F | 64 | 0x0000 | 85 | 0x70A6 | 105 | 0x0000 |
| 21 | Read Only | 45 | 0x9FE0 | 65 | 0x0000 | 86 | 0x0000 | 106 | 0x0000 |
| 22 | 0x3200 | 46 | 0x0072 | 66 | 0x9000 | 87 | 0x0000 | 112 | 0x2000 |
| 24 | 0x086C | 47 | 0x00D3 | 67 | 0x0000 | 89 | 0xF7A1 | 113 | 0x9377 |
| 25 | 0x13BA | 48 | 0x6C0D | 68 | 0x0000 | 90 | 0x3C66 | 114 | 0x26EE |
| 26 | 0x0000 | 49 | 0xD1D5 | 69 | 0x1FFF | 91 | 0x0000 | 115 | 0x0000 |
| 28 | 0x0000 | 50 | 0xF717 | 70 | Read Only | 92 | 0x0000 | 116 | 0x0000 |
| 30 | 0x0000 | 51 | 0x0735 | 71 | 0x0000 | 93 | 0x0000 | 117 | 0x0400 |
| 31 | 0x0000 | 52 | 0x6D72 | 72 | 0x2000 | 94 | 0x0000 | 118 | 0x0000 |
| 32 | 0x0000 | 53 | 0xCD0B | 73 | 0x0000 | 95 | 0xE000 | 122 | 0x46A3 |
| 34 | 0x0740 | 54 | 0xDDAC | 75 | 0x7A81 | 96 | 0x0013 | 123 | 0x0002 |
| 36 | 0x8000 | 55 | 0x15D8 | 76 | 0x64A4 | 97 | 0x0100 | 124 | 0x76B2 |
| 37 | 0x04D5 | 56 | 0x6F82 | 77 | 0x0000 | 98 | 0x0003 | 125 | 0x987F |
| 38 | 0xE000 | 57 | 0xC723 | 78 | 0x0000 | 99 | 0x0237 | 126 | 0xFFFC |
| 39 | 0x0013 | 58 | 0xC7A5 | 79 | 0x0000 | 100 | 0x0000 | 127 | 0x88BE |

Please note that digital registers not listed in the table above are either useless or read only.

# TX Audio

| Register (DEC) | Default Value | Description |
|---|---|---|
| 12<10> | | 0x0 TX Audio On<br>0x1 TX Audio Off |
| 17 | 0x5800 | Settings for digital filters |
| 18 | 0x415C | B06~B02: TX Audio Gain (Digital) |
| 19 | 0x08A0 | Digital limiter used to limit the maximum frequency deviation. Unit: Hz |
| 40<15> | | 0x0 Disable in-band Signal<br>0x1 Enable in-band Signal |
| 40<14:13> | | In-band Signal Type<br>0x0 Voice<br>0x1 DTMF<br>0x2 FSK<br>0x3 SELCALL |
| 40<12:09> | 0x4 | In-band Signal Gain. 0.1x ~ 1.6x |
| 40<07> | | 0x0 Disable sub-audio Signal<br>0x1 Enable sub-audio Signal |
| 40<06> | | Sub-audio Signal Type<br>0x0 CTCSS<br>0x1 CDCSS |
| 40<05:02> | 0x8 | Sub-audio Signal Gain. 0.05x ~ 2x |
| 41 | 0x2050 | B15~B10: TX Deviation Gain. Apply for both in-band signal and sub-audio signal. 0:0.5x, 1:1x, 2:2x, ……, 63:63x |
| 44 | 0x8A2E | TX Audio AGC Settings |
| 45 | 0x1B80 | TX Audio AGC Settings. REG45<11:6> must be the same s REG44<5:0> |
| 107 | 0x3415 | Settings for analog part |

# RX Audio

| Register (DEC) | Default Value | Description |
|---|---|---|
| 12<11> | | 0x0 RX Audio On<br>0x1 RX Audio Off |
| 64 | 0x8000 | Settings for digital filters |
| 65<15:14> | 0x3 | Channel Filter Bandwidth Selection<br>0x0 Auto-selection<br>0x2 Wide Bandwidth 5kHz<br>0x3 Narrow Bandwidth 3kHz |
| 65<12:0> | 0x0 | Limit the output amplitude of RX audio<br>0x0 No limitation |
| 66 | 0xD003 | B12: Enable Voice RX<br>B11: Enable DTMF RX<br>B10: Enable FSKRX RX<br>B09: Enable SELCALL RX<br>B08: Enable CTCSS RX<br>B07: Enable CDCSS RX |
| 72 | 0xA002 | Settings for digital filters |
| 73 | 0x0080 | B03~B00: Digital Volume Control |
| 108 | 0x6927 | B14~B11: Analog Volume Control |

Please note that limiter(REG65<12:0>) for RX audio is a new function in BK4815N. This function is added to limit the unpleasant FM De-mod noise level when there is no wanted signal.

1) To disable this function, please set REG65<12:0>=0x0

2) To enable this function, please tuning REG65<12:0> until the output volume equals to the rated maximum volume

# Automatic Frequency Correction

| Register (DEC) | Default Value | Description |
|---|---|---|
| 69<15> | 0x0 | Disable AFC Function.<br>0: Enable<br>1: Disable |
| 69<14:13> | 0x1 | AFC Gain.<br>0: 2x<br>1: 1x<br>2: 0.5x<br>3: 0.25x |
| 69<12:00> | 0x7FF | AFC Search Range (Unit: Hz)<br>For example, HEX2DEC(0x7FF) = 2047. So the search range is +/-2047Hz. |
| 70 | | B13~B00: Residual Frequency Indicator (complement) |
| 71 | 0x0A19 | B13~B08: SNR threshold for AFC<br>B07: AFC direction<br>B06~B00: RSSI threshold for AFC |

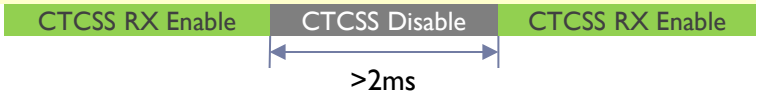
# CTCSS

| Register (DEC) | Default Value | Description |
|---|---|---|
| 36 | | B14~B13: High 2 bits of CTCSS frequency for TX<br>B01~B00: CTCSS phase. 0: 0, 1: 120, 2: 180, 3: 240 |
| 37 | | Low 16bits of CTCSS frequency for TX |
| 40<07:06> | 0x2 | Enable CTCSS transmit |
| 66<08> | | Enable CTCSS receive (Should be enabled for each detection) |
| 89 | 0xF7A0 | Match condition |
| 90 | 0x3C46 | Match condition |
| 91 | | B15~B13: Symbol address of CTCSS frequency for RX<br>B12~B00: 13 bits CTCSS frequency for RX |
| 92 | 0x0000 | B06~B04: Address of found CTCSS. Read only<br>B02~B00: Number of symbols to be searched. 0: 1 symbol 1: 2 symbols 7: 8 symbols |
| 93 | 0x00C0 | B08~B02: Threshold for loss interrupt. The suggest value is 0x30<br>B01~B00: Found CTCSS phase change. 0: 0, 1: 120 or 240, 2: 180 |
| 115 | | B08: Enable CTCSS found interrupt<br>B07: Enable CTCSS loss interrupt |
| 116 | | B08: CTCSS found indicator<br>B07: CTCSS loss indicator |

## TX:

1. Set the phase of CTCSS (REG36<01:00>)
2. Set CTCSS frequency (REG36<14:13> and REG37).
   Equation for CTCSS frequency is
   value =DEC2HEX( Freq/18466*65536*4)
3. Enable CTCSS transmit (REG40<07:06> =0x2)

The time slot between 2 times CTCSS RX enable should > 2ms




## RX:

1. Set the number of symbols to be searched (REG92<02:00>)
2. Set the search table of CTCSS (REG91).
   Equation for REG91<12:00> is
   value =DEC2HEX( Freq/18466*65536*8)
3. Enable CTCSS found interrupt (REG115<08> = 0x1)
4. Enable CTCSS receive (REG66<08> = 0x1)
5. If interrupt is triggered, read REG116. If REG116<8> is 0x1, then CTCSS symbol is detected. Please find the address of detected symbol in REG92<06:04>

# CDCSS

| Register (DEC) | Default Value | Description |
|---|---|---|
| 38 / 39 | | DCS code for TX |
| 40<07:06> | 0x3 | Enable CDCSS transmit |
| 66<07> | | Enable CDCSS receive |
| 94 | 0x8028 | B14~B08: Address of found CDCSS. Read only<br>B02: Phase of found CDCSS. 0: Positive 1: Negative |
| 95 / 96 | | DCS code for RX |
| 97 | New function | B15~B08: Number of symbols to be searched. 0: None 1: 1 symbol 2: 2 symbols<br>B07: Search mode. 0: Both normal code and inverse code 1: Normal code only<br>B06~B00: Symbol address of DCS code for RX |
| 115 | | B05: Enable CDCSS found interrupt<br>B04: Enable CDCSS loss interrupt |
| 116 | | B05: CDCSS found indicator<br>B04: CDCSS loss indicator |
| 123<01:00> | 0x2 | High 2 bits of divide ratio. Equation for divide ratio is value = DEC2HEX(26e6/freq) |
| 124 | 0xF3AC | Low 16 bits of divide ratio. The default CDCSS frequency is 134.4 Hz |

- TX:
  1. Set DCS code (REG38/REG39 )
     (D023N: Reg38=0x0B04, Reg39=0x0E3F)
  2. Enable CDCSS transmit (REG40<07:06> = 0x3)

DCS Code List is given in an excel document in design kit.

- RX:
  1. Set the number of symbols to be searched (REG97<15:08>)
  2. Write REG97<06:00> first, then REG95/REG96 (D023N: Reg95=0x0B04, Reg96=0x0E3F)
  3. Write all CDCSS code in the search table according to step 2 if the symbol numbers to be searched > 1
  4. Enable CDCSS found interrupt (REG115<05> = 0x1)
  5. Enable CDCSS receive (REG66<07> = 0x1 )
  6. If interrupt is triggered, read REG116. If REG116<5> is 0x1, then CDCSS symbol is detected. Please find the address of detected symbol in REG94<14:08>

# SELCALL

| Register (DEC) | Default Value | Description |
|---|---|---|
| 34 | | SELCALL frequency for TX |
| 40<15:13> | 0x7 | Enable SELCALL transmit |
| 66<09> | | Enable SELCALL receive |
| 84 | 0xFC46 | Match condition |
| 85 | 0x78A6 | Match condition |
| 86 | | B15~B12: Symbol address of SELCALLL frequency for RX<br>B11~B00: SELCALL frequency for RX |
| 87 | 0x0000 | B07~B04: Address of found SELCALL symbol<br>B03~B00: Number of symbols to be searched.<br>0: 1 symbol 1: 2 symbols 15: 15 symbols |
| 115<9> | | Enable SELCALL found interrupt |
| 116<9> | | SELCALL found indicator |

- TX:
  1. Set the value of SELCALL frequency (REG34). Equation is value = DEC2HEX(Freq/18466*65536)
  2. Enable SELCALL transmit (REG40<15:13> = 0x7)

- RX:
  1. Set the number of symbols to be searched (REG87<03:00>)
  2. Set the search table of SELCALL frequency (REG86). Equation for REG86<11:00> is value = DEC2HEX(Freq/18466*4096)
  3. Enable SELCALL found interrupt (REG115<09> = 0x1)
  4. Enable SELCALL receive (REG66<09> = 0x1)
  5. If interrupt is triggered, read REG116. If REG116<9> is 0x1, then SELCALL symbol is detected. Please find the address of detected symbol in REG87<07:04>

# DTMF

| Register (DEC) | Default Value | Description |
|---|---|---|
| 24 | | DTMF low band frequency for TX |
| 25 | | DTMF high band frequency for TX |
| 40<15:13> | 0x5 | Enable DTMF transmit |
| 66<11> | | Enable DTMF receive |
| 75 | 0x7A86 | Match condition |
| 76 | 0x6506 | Match condition |
| 77 | | B15~B12: Symbol address of DTMF for RX<br>B11: DTMF band to be wrote in B11~B00 for RX. 0: Low band 1: High band<br>B10~B00: DTMF frequency |
| 78 | | B07~B04: Address of found DTMF symbol<br>B03~B00: Number of symbols to be searched.<br>0: 1 symbol 1: 2 symbols 15: 15 symbols |
| 115<10> | | Enable DTMF found interrupt |
| 116<10> | | DTMF found indicator |

- TX:
  1. Set the low band frequency of DTMF (REG24).
     Equation is value = DEC2HEX(Freq/18466*65536)
  2. Set the high band frequency of DTMF (REG25).
     Equation is value = DEC2HEX(Freq/18466*65536)
  3. Enable DTMF transmit (REG40<15:13> = 0x5)

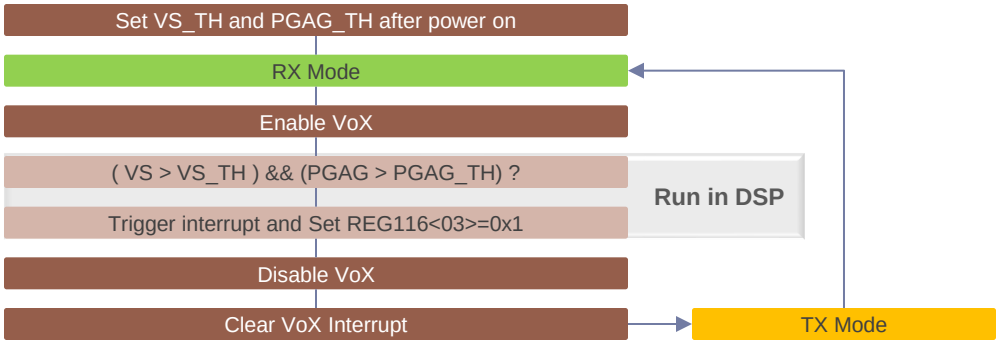
- RX:
  1. Set the number of symbols to be searched (REG78<03:00>)
  2. Set the search table of DTMF (REG77).
     Equation for REG77<10:00> is
     value = DEC2HEX(Freq/4103*4096)
     REG77 should be wrote 2 times for each symbol. One time for low band frequency, another time for high band frequency
  3. Enable DTMF found interrupt (REG115<10> = 0x1)
  4. Enable DTMF receive (REG66<11> = 0x1)
  5. If interrupt is triggered, read REG116. If REG116<10> is 0x1, then SELCALL symbol is detected. Please find the address of detected symbol in REG78<07:04>

# FSK

- To be determined

# VoX

| Register (DEC) | Default Value | Description |
|---|---|---|
| 21 | Read Only | B15~B08: Voice strength indicator from microphone (VS)<br>B05~B00: Gain indicator of audio PGA for microphone (PGAG), depend on TX Audio AGC |
| 22<15> | 0x0 | VoX enable.<br>0: Disable<br>1: Enable |
| 22<14> | 0x0 | Voice Detection Speed.<br>0: Fast<br>1: Slow |
| 22<13:06> | | Voice strength threshold for VoX (VS_TH) |
| 22<05:00> | | PGA gain threshold for VoX (PGAG_TH) |
| 115<03> | | VoX Interrupt Enable.<br>0: Disable<br>1: Enable |
| 116<03> | | VoX indicator<br>0: No<br>1: Yes |




Notes:

1. In TX mode or loop-back mode, if VoX enabled, voice strength will be calculated by DSP, but DSP will not give interrupt.
2. To using VoX function, TX audio PGA must be power up (REG12<10>=0x0)

# Squelch

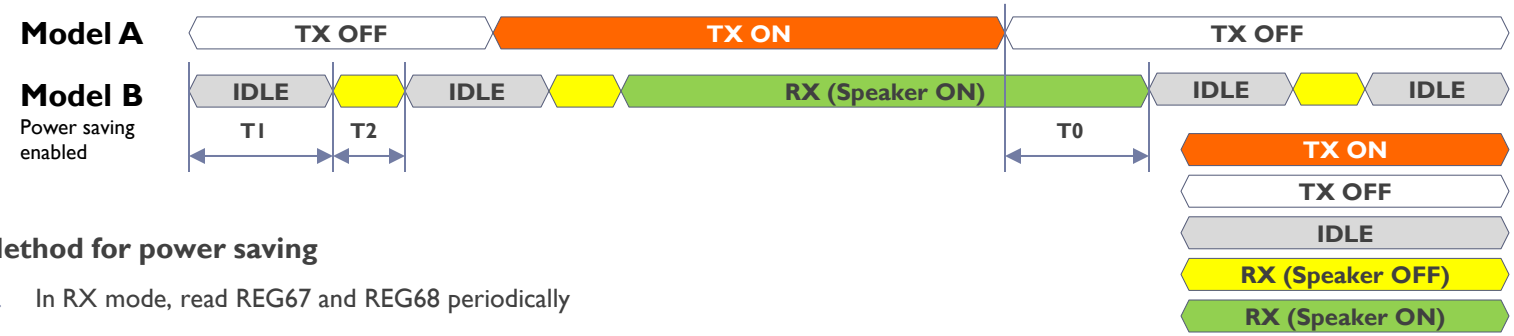
| Register (DEC) | Default Value | Description |
|---|---|---|
| 67<13> | 0x1 | Ex-noise type.<br>0: REG67<12:00> is real-time value<br>1: REG67<12:00> is averaged value |
| 67<12:00> | | Ex-noise indicator |
| 68 | | B15~B14: SNR/RSSI/Ex-noise update period<br>0: 28ms 1: 14ms 2: 7ms 3: 3.5ms<br>B13~B08: SNR indicator<br>B06~B00: RSSI indicator |
| 102<13> | 0x0 | Reference selection for Link or Loss interrupt REG116<06><br>0: Use ex-noise as the reference<br>1: Use RSSI and SNR as the reference |
| 102<12:0> | 0x1E9 | Ex-noise threshold for loss interrupt<br>If REG102<13 is 0x0 and (REG67<12:00>) > (REG102<12:0>), REG116<06> will be 0x1 |
| 115<06> | | Enable Link and Loss interrupt |
| 116<06> | | Link and Loss indicator |

- **For the operation to turn on the speaker, the only method is to read RSSI indicator and Ex-noise indicator.**
  1. If (RSSI > RSSI_TH1) and (Ex-noise < Ex-noise_TH1), there should be a valid signal at wanted channel
  2. The condition in step 1 should last for certain period (>50ms) to avoid wrong operation
- **For the operation to turn off the speaker, there are two method.**
- One method is to read RSSI indicator and Ex-noise indicator. Another method is using interrupt.
  1. If (RSSI < RSSI_TH2) or (Ex-noise > Ex-noise_TH2), the valid signal at wanted channel disappear
  2. The condition in step 1 should last for certain period (>50ms) to avoid wrong operation
- Another method is using interrupt
  1. Set REG102<12:0> to EX-noise_TH2 and REG115<06>=0x1
  2. If the valid signal at wanted channel disappear, interrupt will be triggered

To assure a certain hysteresis, make sure
(RSSI_TH2 < RSSI_TH1) and (Ex-noise_TH2 > Ex-noise_TH1)

# Power Saving

| Register (DEC) | Default Value | Description |
|---|---|---|
| 11 | | For VCO calibration (B12 and B15) |
| 12 | | B15~B12: Disable analog part |
| 67 | | B12~B00: Ex-noise indicator |
| 68 | | B06~B00: RSSI indicator |
| 112 | | For digital reset (B13 and B15) |

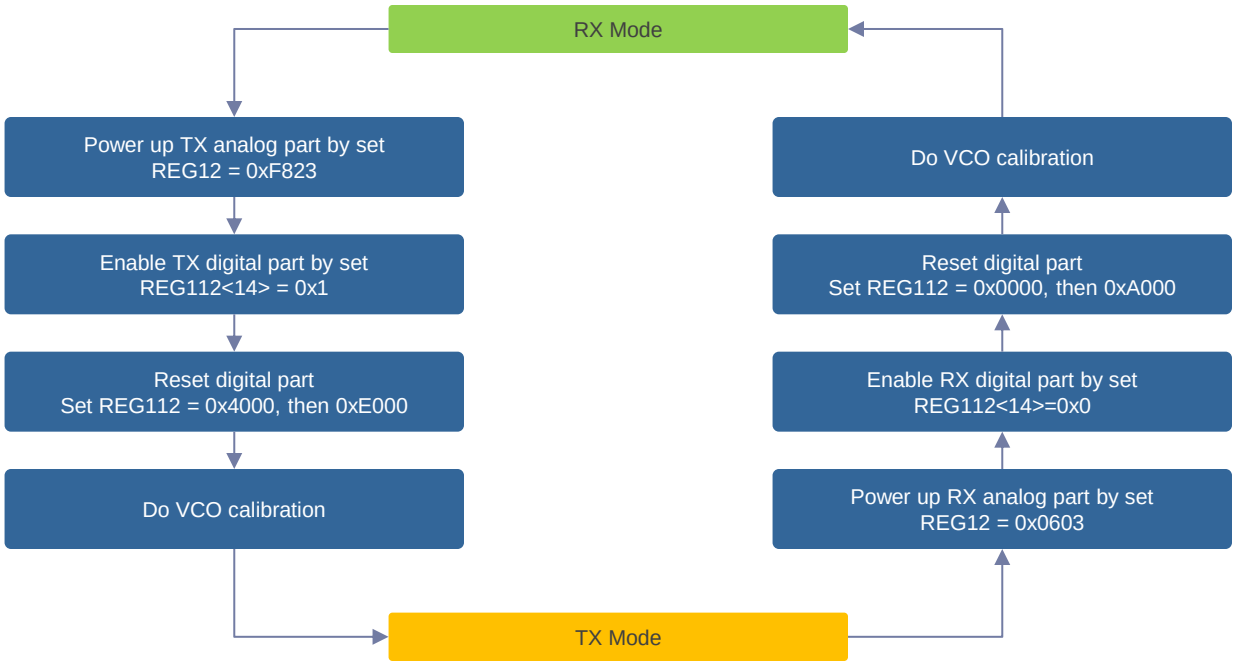



- **Method for power saving**
  1. In RX mode, read REG67 and REG68 periodically
  2. If (RSSI < RSSI_TH) and (Ex-noise > Ex-noise_TH)
  3. And the condition in step 2 last for a certain period T0, then enter idle mode(set REG12=0xFFFF). Else, go to step 1
  4. Wait for a period T1
  5. Power up RX analog part (Set REG12=0x0E2B) and do VCO calibration
  6. Reset digital part (Set REG112 to 0x0000, then set REG112 to 0xA000)
  7. Wait for a certain period T2
  8. Read REG67 and REG68
  9. If (RSSI < RSSI_TH) and (Ex-noise > Ex-noise_TH), then enter idle mode(set REG12=0xFFFF) and go to step 4. Else, open the speaker(set REG12<11>=0x0 )and go to step 1

# TX/RX Mode Switch

| Register (DEC) | Default Value | Description |
|---|---|---|
| 11 | | For VCO calibration (B12 and B15) |
| 12 | | B15~B12: Disable analog part |
| 112 | | For digital reset (B13 and B15) |

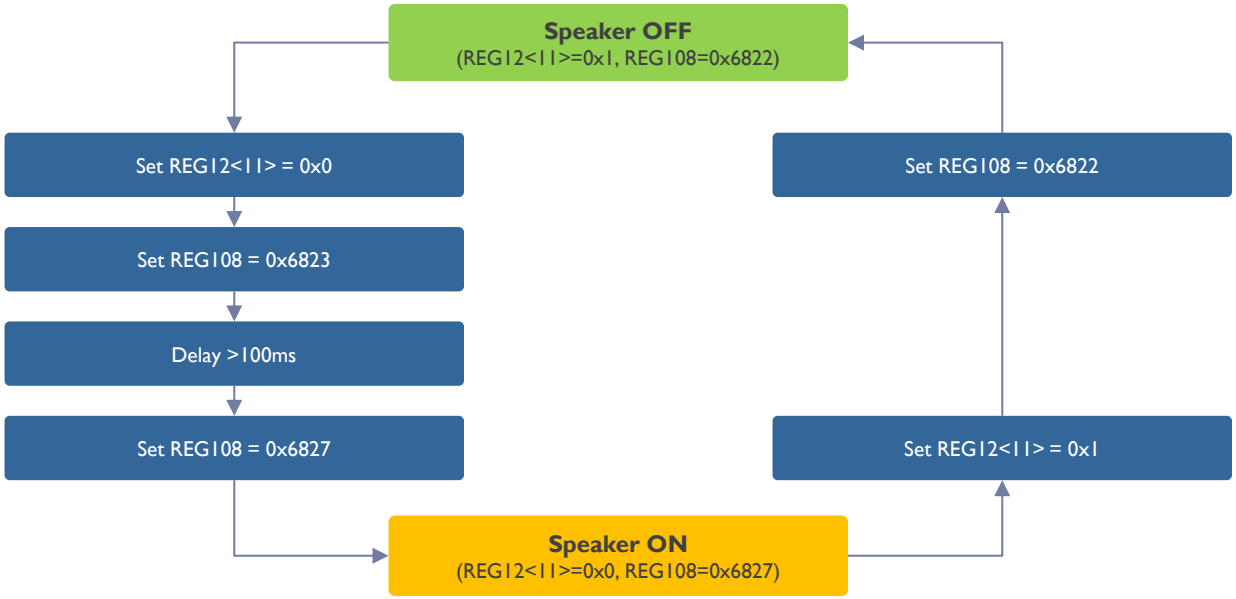
- Mode switch between TX mode and RX mode is much easier compared with BK4811B/BK4813



# Pop Sound

| Register (DEC) | Default Value | Description |
|---|---|---|
| 12<11> | | Disable analog part of RX audio<br>0: Enable<br>1: Disable |
| 108 | 0x6827 | B02: Enable large current driving. 0: Small current driving 1: Large current driving<br>B00: Enable driver bias. 0: Disable bias 1: Enable bias |

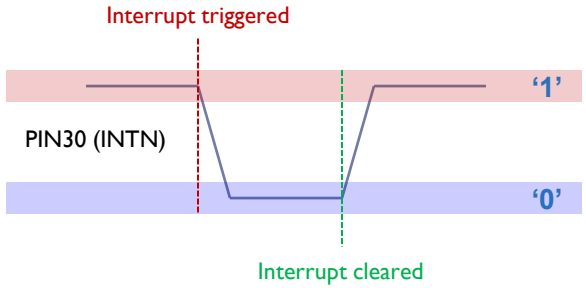
- If don't take special operation, there will be pop-sound when RX audio on or off.
- Method to avoid pop sound is shown below




Make sure that the AC coupling capacitor at PIN 8(EARO) is not less than 1uF. This is very important to avoid pop-sound.

# Interrupt

- Besides 3-wire SPI (SCK, SCN and SDATA), there is a fourth PIN connect to the MCU. That is PIN 30 (INTN) which delivers interrupt signal from DSP in BK4815N to the MCU.
- For normal case, PIN 30 is of high level. When a interrupt is triggered, PIN 30 will be low level until the interrupt is cleared.




- Method to clear interrupt
  - Write corresponding bit to 0x1
  - For example, if DTMF interrupt is triggered, REG116<10> should be wrote to 0x1 to clear the interrupt.

| REG (DEC) | Description |
|---|---|
| 115 | B15: Main switch. 0: Disable all interrupt 1: Enable all interrupt<br>B14: Enable FSK send done interrupt<br>B13: Enable FIFO need fill interrupt<br>B12: Enable FSK head found interrupt<br>B11: Enable FIFO need read interrupt<br>B10: Enable DTMF found interrupt<br>B09: Enable SELCALL found interrupt<br>B08: Enable CTCSS found interrupt<br>B07: Enable CTCSS loss interrupt<br>B06: Enable Link and Loss interrupt<br>B05: Enable DCS found interrupt<br>B04: Enable DCS loss interrupt<br>B03: Enable VoX interrupt<br>B01: Enable FSK receive done interrupt |
| 116 | B15: Clear all interrupt<br>Write to 0x0: Invalid operation<br>Write to 0x1: Clear all interrupt<br>B14: FSK send done indicator<br>B13: FIFO need fill indicator<br>B12: FSK head found indicator<br>B11: FIFO need read indicator<br>B10: DTMF found indicator<br>B09: SELCALL found indicator<br>B08: CTCSS found indicator<br>B07: CTCSS loss indicator<br>B06: Link and Loss indicator<br>REG70<14>=0x0: Loss REG70<14>=0x1: Link<br>B05: DCS found indicator<br>B04: DCS loss indicator<br>B03: VoX indicator<br>B01: FSK receive done indicator |

# GPIO

| Register (DEC) | Default Value | Description |
|---|---|---|
| 117<05:03> | | GPIO1 mode selection<br>0: Input<br>1: Output low '0'<br>2: Output high '1'<br>3~7: Invalid |
| 117<02:00> | | GPIO0 mode selection<br>0: Input<br>1: Output low '0'<br>2: Output high '1'<br>3: CTCSS square wave<br>4: DCS code<br>5~7: Invalid |
| 118 | | B01: GPIO1 input value<br>B00: GPIO0 input value |

- There are 2 GPIO PINs, PIN28(GPIO0) and PIN29(GPIO1)
- DCS code or CTCSS signal(square wave) can be send to MCU through GPIO0

# Frequency Settings

| Register (DEC) | Description | Typical value |
|---|---|---|
| 04<08:07> | DIV ratio from VCO to LO | 0x0 for 446.00625MHz |
| 13<01> | IF selection (0x1: 187kHz 0x0: 88kHz) | 0x1 for 137kHz |
| 113 | High 16 bits for channel frequency | 0x893B for 446.00625MHz |
| 114 | Low 16 bits for channel frequency | 0x91B9 for 446.00625MHz |
| 125 | IF settings for digital mixer | 0xED69 for 446.00625MHz and 137kHz IF |
| 126 | High 16 bits of IF settings for PLL | 0xFFF5 for 446.00625MHz and 137kHz IF |
| 127 | Low 16 bits of IF settings for PLL | 0x3568 for 446.00625MHz and 137kHz IF |

$$N_{RF} = Round(\frac{f_{wanted} \times DIV \times 2^{24}}{f_{XTAL}})$$

$$REG113 = High\ 16\ bits\ of\ Hex(N_{RF})$$

$$REG114 = Low\ \ 16\ bits\ of\ Hex(N_{RF})$$

$$REG125 = Round(\frac{f_{IF} \times 2^{16} \times 88}{f_{XTAL}})$$

$$N_{IF} = 2^{32} - Round(\frac{f_{IF} \times DIV \times 2^{24}}{f_{XTAL}})$$

$$REG126 = High\ 16\ bits\ of\ Hex(N_{IF})$$

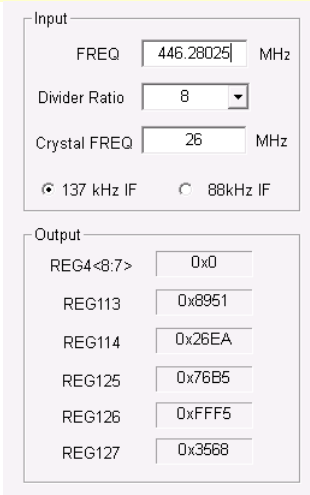
$$REG127 = Low\ \ 16\ bits\ of\ Hex(N_{IF})$$

$f_{wanted}, f_{IF}, f_{XTAL}$ are in unit Hz.

*These equations apply for both narrow band (12.5kHz channel spacing) and wide band (25kHz channel spacing).*

IF can either be set to 137kHz or 88kHz. Other IF value are not supported.

An EXE calculator is given in the design kit.



# VCO Coverage

| Band | LO Frequency Range | REG4<8:7> | DIV |
|---|---|---|---|
| 1 | 383MHz ~ 590MHz | 0x0 | 8 |
| 2 | 255MHz ~ 394MHz | 0x2 | 12 |
| 3 | 192MHz ~ 295MHz | 0x1 | 16 |
| 4 | 128MHz ~ 197MHz | 0x3 | 24 |

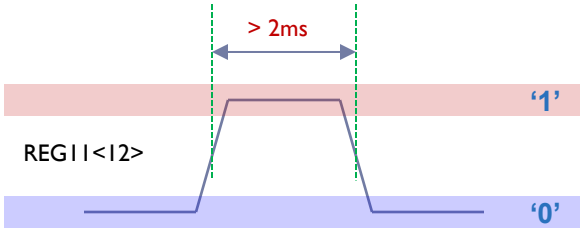
**Notes:**

1. All these values are typical values
2. Frequency range may varies chip by chip
3. Frequency range will goes downward when temperature increase, and vice versa
4. Both lower boundary and upper boundary may vary ±1% considering above 2 factors.

# VCO Calibration

- **VCO Calibration should be executed at each case below:**
  - Initialization after power-on
  - Press the PTT button (RX to TX)
  - Release the PTT button (TX to RX)
  - Channel switch

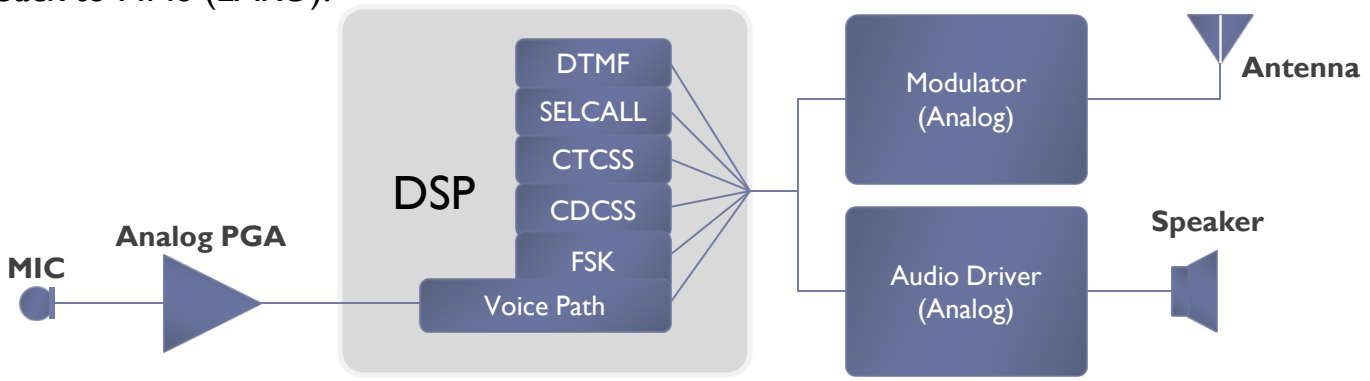
- **Procedure of VCO Calibration**
  1. Set REG11<12>=0
  2. Delay 2ms
  3. Set REG11<12>=1
  4. Delay 1ms
  5. Set REG11<12>=0



# Loop Back Mode

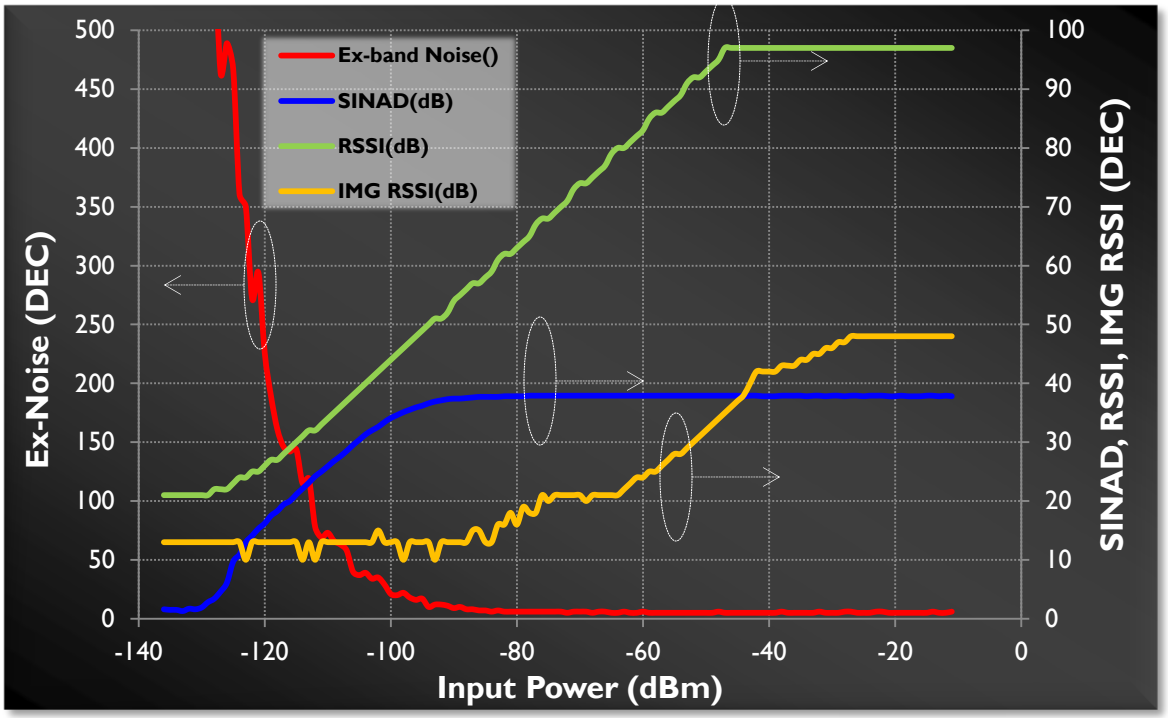
| Register (DEC) | Default Value | Description |
|---|---|---|
| 117<09> | | Loop Back Enable. 0: Disable, 1: Enable |
| 117<08:06> | | Selection of Loop Back Signal<br>0: DCS<br>1: CTCSS<br>2: SELCALL<br>3: DTMF<br>4: FSK<br>5: Voice<br>6: FSK AIR<br>7: Constant 0 |

- Co-existence of TX Voice and Loop Back Signal
  - To have this feature, both TX audio and RX audio should be power up (REG12<11:10> = 0x0)
  - Even if the transmission of TX Voice is ongoing, DTMF/SELCALL/FSK/CTCSS/DCS signals can also be loop-back to PIN8 (EARO).



# SINAD, RSSI, Ex-Noise vs. Input Power

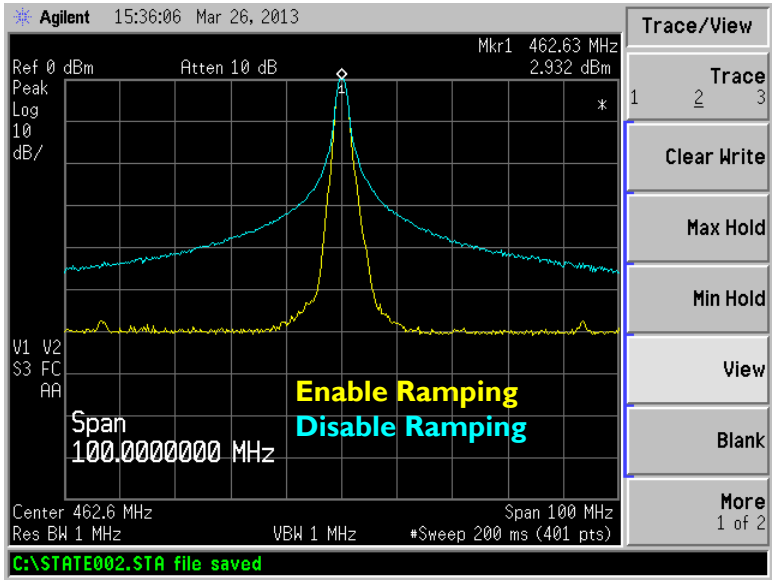
- **RSSI: Received signal strength indicator REG68<06:00>**
- **Ex-Noise: Noise strength of integration from 3kHz~18kHz REG67<12:00>**
  - **If set REG67<13>=0x0, then REG67<12:00> is real-time value**
  - **If set REG67<13>=0x1, then REG67<12:00> is averaged value**
- **IMG RSSI: Signal strength indicator at image frequency (fwanted-2xIF) REG100<06:00>**
  - **IMG RSSI detection should be enabled by set REG100<07>=0x1**




**Indicators versus Input Power**

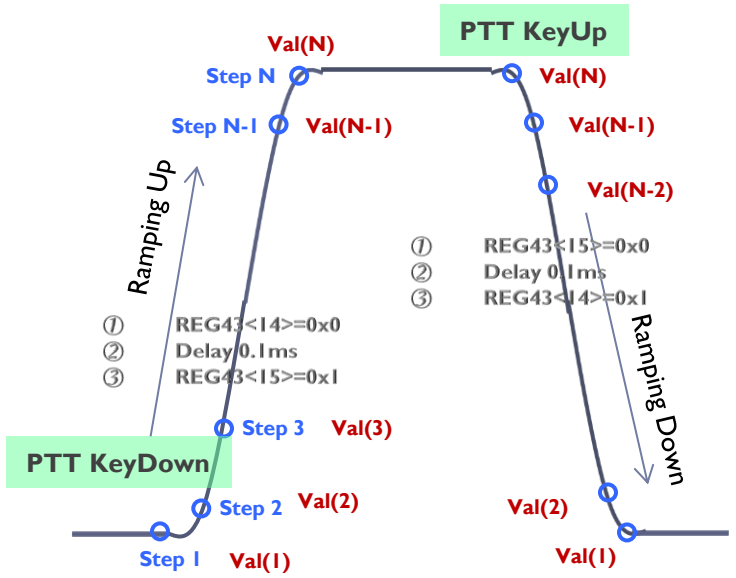
# TX Ramping

| Register (DEC) | Default Value | Description |
|---|---|---|
| 109<12> | 0x0 | Enable Ramping Function<br>0: Disable<br>1: Enable |
| 42 | | B15~B10: Ramping Step<br>B09~B00: Ramping value for each step<br>Should be wrote into BK4815N at register initialization stage if ramping function is preferred. |
| 43 | | B15: Enable Ramp-up<br>B14: Enable Ramp-down<br>B05~B03: Ramp-up speed. 0: 0.08ms 1: 0.16ms 7: 10.27ms<br>B02~B00: Ramp-down speed. 0: 0.08ms 1: 0.16ms 7: 10.27ms |




Ramping Effect

Spectrum Analyzer max-hold
Up to thousand times PTT Up/Down

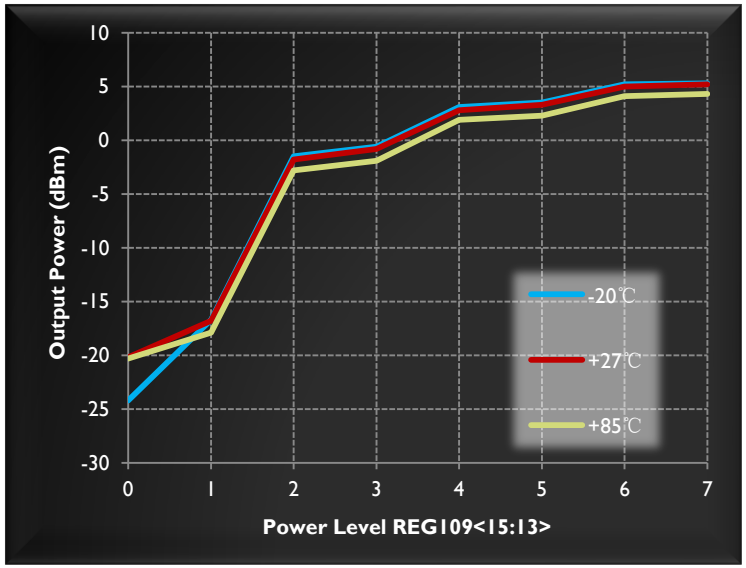



Transient Power Waveform

Ramping array is given in an excel document in design kit.

# TX Output Power

- **REG109<15:13>** can be used to tuning the output power
- The output power ranges from -20dBm to +5dBm




**Output Power versus REG109<15:13>**

# RX AGC

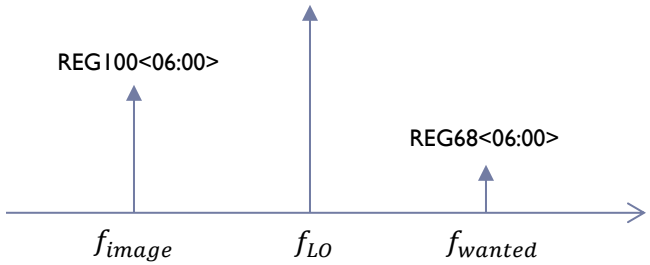
| Register (DEC) | Default Value | Description |
|---|---|---|
| 103<15> | 0x0 | Disable AGC Function.<br>0: Enable<br>1: Disable |
| 103<14:8> | 0x43 | RSSI Offset |
| 103<04> | 0x1 | LNA Gain Control.<br>0: Low Gain<br>1: High Gain |
| 103<02:00> | 0x7 | IF PGA Gain Control.<br>0: 0dB<br>1: 3dB<br>……<br>7 :21dB |

# Image Interference Rejection

| Register (DEC) | Default Value | Description |
|---|---|---|
| 14<10> | 0x0 | LO location. 0: Low side, flo < fwanted, 1: High side, flo > fwanted |
| 68<06:00> | | Received signal strength indicator at wanted channel |
| 100<07> | | Enable image RSSI detection. 0: Disable 1: Enable |
| 100<06:00> | | Received signal strength indicator at image frequency |
| 125 / 126 /127 | | Should be calculated using equations in ***Frequency Settings*** section |

- The method to avoid image cross-talk is shown below:

(Normal state: REG113/REG114 = fwanted, REG14<10>=0)




1. Read wanted signal strength REG68<6:0>, record as RSSI_W
2. Read image signal strength REG100<6:0>, record as RSSI_I
3. If ( RSSI_I > RSSI_W + Delta ) && REG14<10>==0
   set REG113/REG114 = fwanted + 2 x IF and REG14<10> = 1
   (REG113=0x8951, REG114=0x26EA, REG14<10>=1, for fwanted=446.00625MHz / IF=137kHz)
4. Else if (RSSI_I > RSSI_W + Delta ) && REG14<10>==1
   set REG113/REG114 = fwanted and REG14<10>=0
   (REG113=0x893B, REG114=0x91B9, REG14<10>=0 for fwanted=446.00625MHz / IF=137kHz)

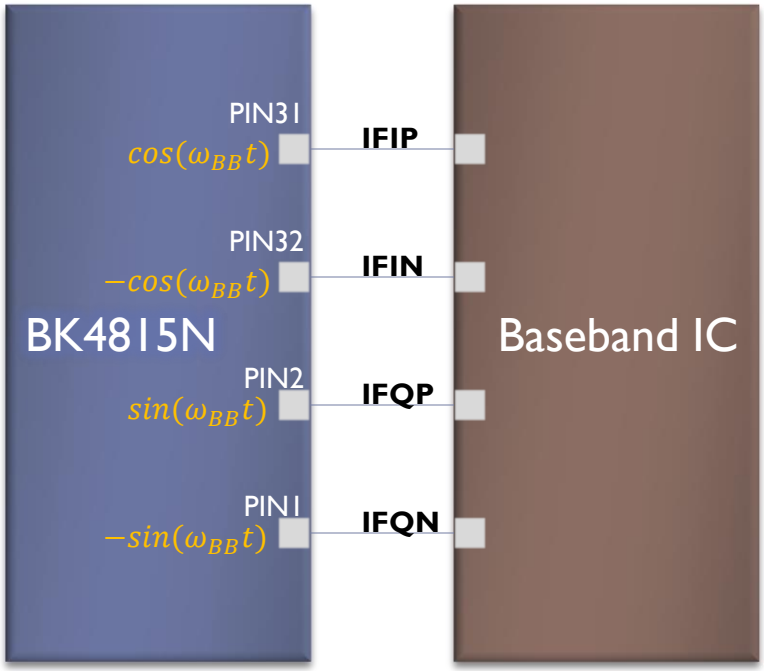
Delta is a constant value that should be less than 40.

# Channel Spacing

- The frequency resolution of BK4815N is less than 1Hz. So, BK4815N can work at any frequency ranges from 128MHz ~ 590MHz.
- For 25kHz channel spacing and wide-band application(Max. Deviation 5kHz), REG1<15> should be 0x1. If better voice quality(High SINAD) is preferred, REG65<15:14> should be 0x2. If better anti-interference performance(Better ACS, IMD and Blocking) is preferred, REG65<15:14> should be 0x3.
- For 12.5kHz channel spacing and narrow-band application(Max. Deviation 2.5kHz), REG1<15> should be 0x0. If better voice quality(High SINAD) is preferred, REG65<15:14> should be 0x2. If better anti-interference performance(Better ACS, IMD and Blocking) is preferred, REG65<15:14> should be 0x3.
- For 6.25kHz channel spacing and narrow-band application(Max. Deviation 1.25kHz), REG1<15> should be 0x0 and REG65<15:14> should be 0x3.

# Digital Walkie-Talkie

- **Path for digital walkie-talkie can be enabled by set**
  1. REG12<05>=0 and
  2. REG15<06>=1
- **Other registers are the same with that in analog mode**




| Register (DEC) | Default Value |
|---|---|
| 46 | 0x0072 |
| 47 | 0x00D3 |
| 48 | 0x6C0D |
| 49 | 0xD1D5 |
| 50 | 0xF717 |
| 51 | 0x0735 |
| 52 | 0x6D72 |
| 53 | 0xCD0B |
| 54 | 0xDDAC |
| 55 | 0x15D8 |
| 56 | 0x6F82 |
| 57 | 0xC723 |
| 58 | 0xC7A5 |
| 59 | 0x2206 |
| 60 | 0x721B |
| 61 | 0xC235 |
| 62 | 0x1141 |

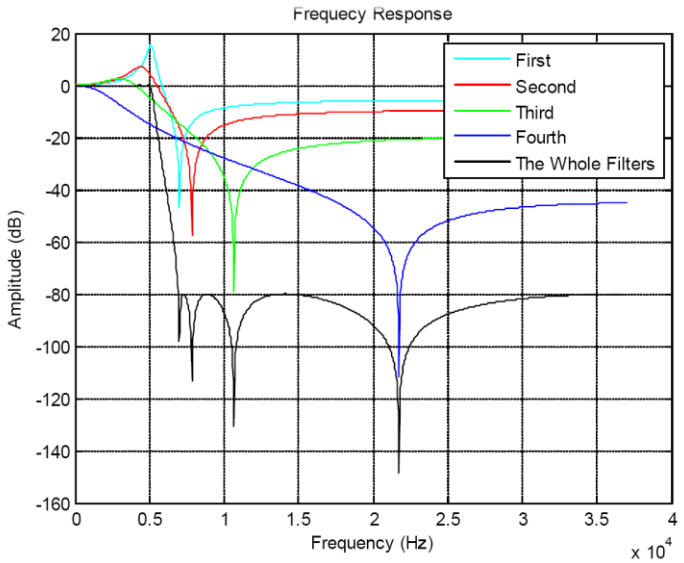
# Digital Walkie-Talkie

- Equation to calculate the frequency of BB signal

$$f_{BB} = \frac{HEX2DEC(\text{REG62} < 15:8 >) \times 256 \times f_{XTAL}}{65528 \times 352}$$

*So, 1 LSB is about 288.565Hz. If REG62<15:8> = 0x11, then the frequency of BB signal should be 4905.606Hz.*

- There is a 4 stages cascade IIR filter. The frequency response of this IIR filter is shown in the figure below




| Register (DEC) | Default Value | Description |
|---|---|---|
| 62<15:8> | | Set the output frequency of BB signal. |
| 62<7:6> | | Gain settings before second mixer |
| 62<05:04> | 0x0 | Set the frequency of clock.<br>0: 73.864kHz<br>1: 73.864kHz * 2<br>2: 73.864kHz * 4<br>3: 73.864kHz * 8 |
| 62<03> | | Clock Enable.<br>0: Disable<br>1: Enable |
| 62<02:00> | 0x7 | IF PGA Gain Control.<br>0: 0dB<br>1: 6dB<br>……<br>7 :42dB |

# Hardware Design

- Decoupling capacitor should be placed as close to the IC as possible
- The inductor between LNA input and ground can not be omitted. Without this inductor, the linearity of the receiver will degrade
- Tolerance of XTAL should be within +/-2.5ppm
- Adjustable capacitor or adjustable resistor should connect to PIN 4(XO) rather than PIN5(XI)
- Ground plane at the PCB bottom layer should be as large as possible
- No routing of noisy trace such as supply at the bottom layer under the antenna matching or RF matching

# Beken Corporation

## Disclaimer



Website: www.bekencorp.com
Email: info@bekencorp.com

Shanghai Headquarters:
Building 41, Capital of Tech Leaders, 1387 Zhangdong Road, Zhangjiang High-Tech Park,
Pudong New District, Shanghai, China
Phone: 86-21-51086811, 60871276
Fax: 86-21-60871277
Postal Code: 201203

Shenzhen Branch:
Room 310, HKUST SZ IER Building, No. 9 Yuexing 1st Rd.,
Nanshan Hi-Tech Park, Shenzhen, China
Phone: 86-755-2655 1063
Postal Code: 518057

Taipei Branch:
2F.-1, No.49, Ln.35, Jihu Rd., Neihu Dist.,
Taipei City, Taiwan
Phone: 886-2-26275780