Selected Topics in RF Coplanar Probing

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***Abstract*—The RF coplanar probe is a popular tool for launching high-frequency signals onto and off of a wafer. Physically contacting the die, it establishes a crucial link between the test system and wafer. Their proper use permits a higher degree of measurement accuracy compared to test fixturing. To augment the reader's understanding, this tutorial reviews selected issues related to the design, construction, characterization, selection, calibration, and repeatability of RF on-wafer coplanar probes.**

***Index Terms*—Coplanar probes, device characterization, modeling, RF on-wafer measurements.**

I. Introduction

WHILE THE digital signal processing (DSP) section of a wireless handset holds thousands of transistors, the biggest challenge in a wireless handset design is often the RF section. The problem usually cited is a lack of computer-aided design (CAD) models to accurately predict the RF integrated circuit's (RFIC) performance [1]. When an RF problem occurs in the design, it is usually attributed to the CAD model, its theoretical basis being drawn into question. Yet shortcomings in the RF performance of a die are just as easily due to the RF measurements used to generate the models as to the models themselves. Recently, RF on-wafer probing has extended beyond RFICs into the world of high-speed digital integrated circuits (ICs) where clocks speeds have exceeded 1 GHz. These trends in digital and RFICs emphasize the need for reliable on-wafer RF measurements.

Twenty years ago, an RFIC wafer was characterized by mounting a single die into a test fixture [see Fig. 1(a)]. The fixture's effects were mathematically deembedded to uncover the die's RF performance. When the RF quantities under study are extremely small, such as in device modeling, fixture deembedding becomes a challenge. Compared to fixturing, coplanar probes are simpler to use and easier to calibrate [see Fig. 1(b)]. In general, RF measurements using coplanar probes produce more reliable device measurements. This, in turn, leads to better-designed RFICs and monolithic microwave integrated circuits (MMICs), increasing the chances of a design's first-pass success. To employ coplanar probes effectively, it helps to understand the fundamental nature of the RF on-wafer coplanar probe. With this in mind, this tutorial reviews selected aspects of RF coplanar probes such as their design, construction, selection, characterization, and use.

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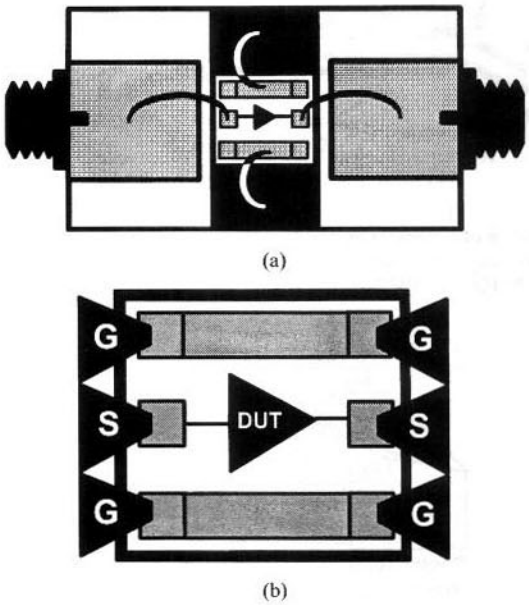

Fig. 1. Two ways to RF measure a single die. (a) Mounting it in a test fixture. (b) Probing it on-wafer with coplanar probes.

II. Coplanar-Probe Construction

The fundamental role of the coplanar probe is to transition the RF signal from one transmission medium to another. For instance, the test cable may be coaxial or rectangular waveguide, while the wafer has either microstrip or CPW lines. Two basic factors govern an effective RF transition. First is an impedance transformation from one characteristic impedance Z_0 to another. Secondly, the electromagnetic (EM)-field pattern is transformed from one mode to another. Carefully designing with these two criteria in mind assures a successful transition. It is worth noting that both ends of the transition can have $Z_0 = 50\ \Omega$, in which case, transforming the EM-field pattern is the goal.

Modern coplanar probes house not one, but a series of RF transitions within the single assembly. Shown in Fig. 2 is a common commercial coplanar probe [2]. To better understand its RF behavior, the probe can be divided according to RF transitions at: 1) the test system interface; 2) transitions within the probe, such as from coaxial to coplanar waveguide (CPW); and 3) from the probe tip to the device-under-test (DUT) on the wafer. These transitions are discussed below.

A. Test System-to-Probe Interface

When both the test system and probe have the same connector, making a connection is easy. The frequency of operation determines the type of connector on the test system. Below 34 GHz, a coaxial cable is commonly used to connect the test system and probe, while in the 34–65 GHz range, it can either

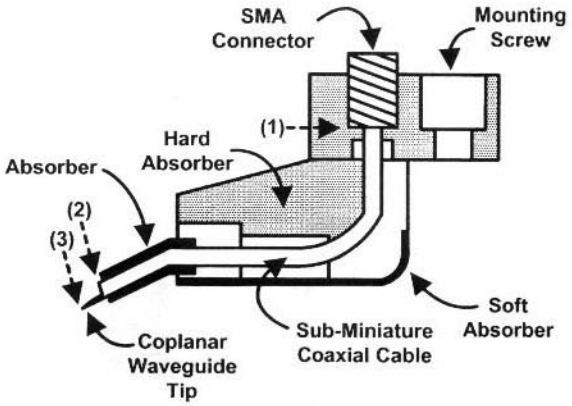

Fig. 2. Cross section of a coplanar probe revealing three transitions. (1) SMA or K connector-to-1 mm subminiature coaxial cable. (2) Subminiature coaxial cable to CPW probe tip. (3) CPW probe tip to the wafer's probe pads.

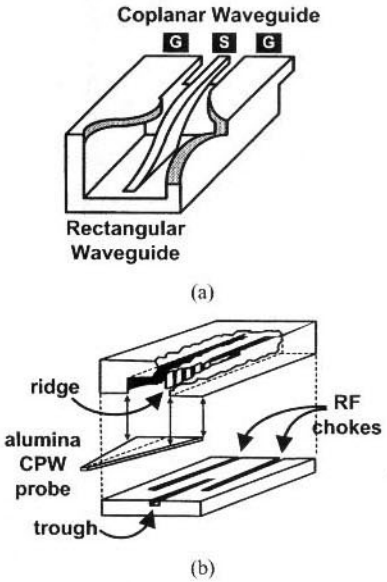

Fig. 3. Two mechanical assemblies to transition the rectangular waveguide to the CPW. (a) Finline transitions G–S–G CPW to rectangular waveguide. The CPW"s grounds contact the waveguide walls while the signal line contacts the fin. Employing a: (b) ridge-trough transition is similar.

be a coaxial cable or rectangular waveguide. Above 65 GHz, a long length of coaxial cable becomes prohibitively lossy. Millimeter-wave propagation over such lengths requires rectangular waveguide. A transition from rectangular waveguide to the probe's subminiature coaxial cable can be achieved within the probe [3]–[5]. However, directly transitioning from rectangular waveguide to CPW eliminates the additional transition from coaxial to CPW. To directly transition, convert the rectangular waveguide's transverse electric (TE_{10}) mode to the TEM mode of the CPW. Rectangular waveguide-to-CPW transitions are accomplished with either finline [6], [7] or ridge trough [8]–[10] structures (see Fig. 3). In the latter, the ridge splits and rotates the TE_{10} field to TEM. Fig. 4 shows how the ridge trough smoothly rotates the TE_{10} waves of the rectangular waveguide to the opposing planar electric fields of the CPW. Rather than using a rectangular waveguide-to-CPW transition within the probe, another option is to transmit the RF down a long coaxial line at a lower frequency and then up-convert it at the probe tip near the DUT. This approach will be discussed later.

B. RF Transitions Within the Probe

The probe houses either a 20- or 31-mil-diameter subminiature coaxial line to minimize insertion loss, as well as maintain a small probe size. One end of the subminiature line connects to the test system. 1.0, 2.4, or 3.5 mm are typical external connector diameters. A change in diameter (see (1) in Fig. 2) requires a reducer. The other end of the probe's subminiature line connects to the CPW probe tip (see (2) in Fig. 2), calling for a coaxial-to-CPW transition [11], [12]. The CPW tips are soldered to the subminiature coaxial line, while the other end of the tips contacts the wafer's probe pads (see Fig. 5). Electrically, the CPW transforms the fields from the diameter of the subminiature coaxial line to the pitch of the wafer probe pads. The width of the CPW signal probe, as well as the gap spacing between ground and signal are designed to yield a 50-Ω characteristic impedance. Tapering the CPW offers the smoothest way to transition the EM fields from coaxial to CPW [13]. A taper along the length slowly transitions from the coaxial cable diameter to the probe-pad pitch. An ideal taper has a constant 50-Ω impedance throughout [14]. A number of tapering schemes are available (linear, exponential, Klopfstein, etc.), all with the objective of maintaining a constant characteristic impedance Z_0 of 50 Ω or minimizing the voltage standing-wave ratio (VSWR) [15]. Designing a probe tip that is sufficiently long with respect to a wavelength allows the probe-tip-to-probe-pad reference plane to be better defined after calibration. When designing the CPW tips, attenuation along the CPW is principally due to skin loss and radiation. As a rule-of-thumb, the probe's skin loss varies as $\sqrt{f}/w$ (dB/mm) where f is the frequency and w is the width of the CPW's center conductor. The CPW's radiation loss varies as $f^3 \bullet w^2$ (dB/mm), although radiation loss is minor compared to skin loss. Mechanically, tapering schemes are not as important as adequate, equal, and repeatable force from each tip. Fabrication tolerances for the CPW tips often determine which probe tip scheme shown in Fig. 5 is most practical. Compared to CPW tips, the backside ground plane of a microstrip tip prevents the signal line from coupling to the wafer surface, shielding the signal tip from the wafer.

Early approaches to fabricating probe tips involved thin film depositing gold CPW lines on a thin alumina substrate. The CPW lines were long enough ($\sim$17 mm) to provide some flexibility so that the alumina would not crack when contacting the wafer. A lack of flexibility causes easy breakage, a statement true of any probe design. The CPW tips found in modern probes are thin metal blades, either machined or laser etched from a sheet of beryllium copper (BeCu) or tungsten (W) and gold plated. The CPW lines can be mounted to the subminiature coaxial line in a number of ways (see Fig. 6). Flexible BeCu keeps the CPW tips from digging into the die's probe pads, optimal for probing gold pads on fragile GaAs wafers. Not only is BeCu flexible, it presents a low contact resistance. Tungsten tips are firmer to break through oxide on aluminum probe pads. During test, aluminum oxide buildup can vary the contact resistance measurement. Furthermore, the contact resistance of W

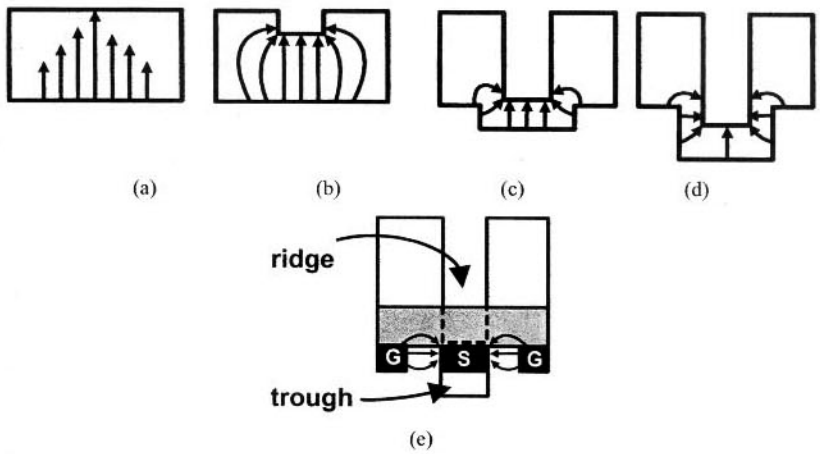

Fig. 4. Electric-field patterns in a ridge-trough transition. (a) Starting with a TE_{10} rectangular waveguide ($Z_0 = 500\ \Omega$) (b) introduce a quasi-TEM ridge, (c) next introduce a trough, (d) increase the ridge-trough dimensions, and (e) finally, arrive at a TEM CPW mode of $Z_0 = 50\ \Omega$.

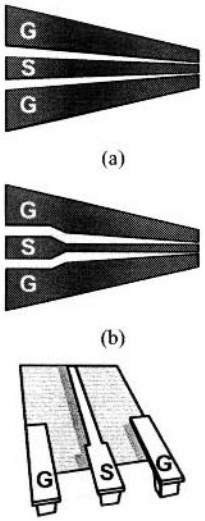

Fig. 5. CPW probe tip transitions from the subminiature coaxial cable to the pitch of the wafer probe pads. (a) Smooth transition, commonly thin-film deposited on an alumina substrate. (b) Signal blade, which abruptly transitions from a coaxial center pin. (c) Microstrip-to-CPW probe tip deposited on a thin polymide film.

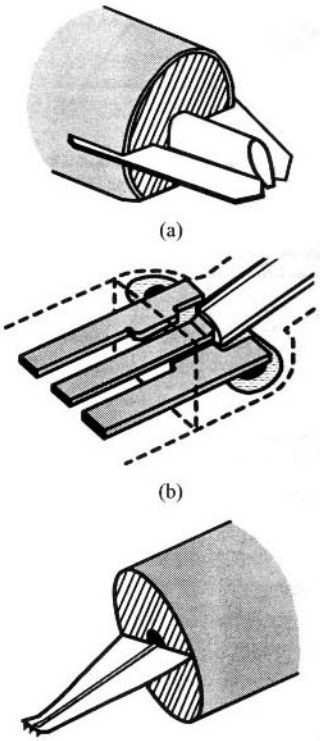

Fig. 6. Three ways to mount CPW probes to the probe's subminiature coaxial line. (a) Two ground blades are held in place by the coaxial dielectric and soldered to the outside of the coaxial shield. The center conductor of the coax serves as the CPW's signal probe. (b) The coaxial signal line is soldered to a CPW blade, while the grounds are mounted to a cross bus from behind. (c) A flexible polymide holds two metal layers with a ground plane on the bottom and a microstrip-to-CPW transition on top.

tips increases with use. With either BeCu or W, the contact pressure of the probe on the wafer has a significant effect on the probe's life span. Gold plating the probe tips reduces skin-effect loss. Nickel underplating keeps the gold from rubbing off, yielding longer probe life. On the polymide tips, a microstrip line transitions to CPW and bumps to contact the wafer probe pads.

C. From the Probe Tips to the On-Wafer DUT

The act of calibration defines the reference plane at the probe tips. Unfortunately, placing the probes directly on the DUT is not possible, requiring probe pads and interconnecting lines. To measure, the reference plane must be shifted from the coplanar probe tips to the DUT plane, illustrating the importance of deembedding, Fig. 7 plots how inductance in the probe pads and interconnecting lines affects the f_T of an active device [16]. There are two transitions to deembed. First is the probe tip-to-wafer probe-pad transition, which is difficult because the probe pad electrically interacts with the probe. Beyond the pads are interconnecting lines leading to the DUT. The second RF transition occurs where the interconnecting lines meet the DUT. The probe pads and interconnects can have parasitics larger than the DUT itself.

Fig. 8 shows an equivalent circuit of a probe-pad stub with and without the probe contacting it. Typical parasitic values on GaAs range from L_{st}, L_{pr}, L_m = 0.2 pH–1.2 pH, R_{st}, R_{pr} = 0.01 Ω–0.2 Ω, G_{st} = 0.2 mS–0.3 mS, C_{st}, C_{pr}, C_m = 0.1 fF–6 fF [17], [18]. In general, the values depend

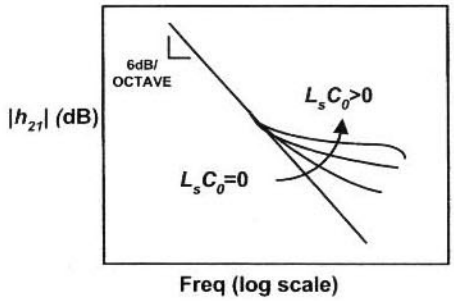

Fig. 7. Resonance between the series inductance of the probe pads and interconnects L_s and a transistor's output capacitance C_0 affects the high-frequency gain h_{21} measurement used to determine f_T.

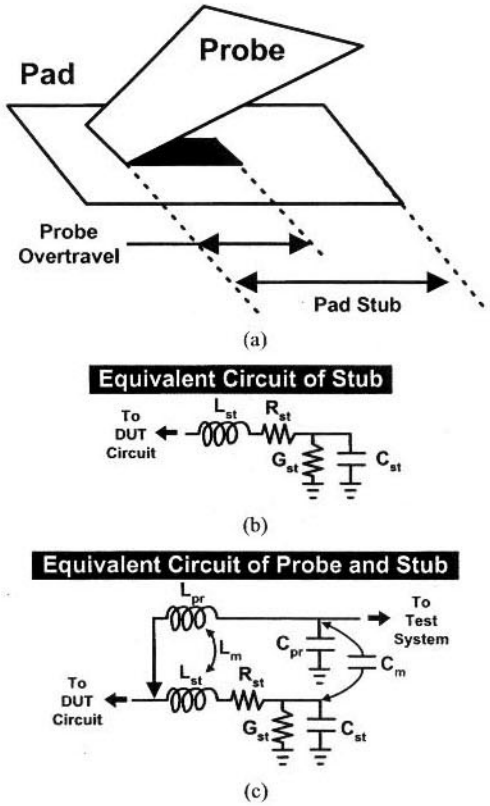

Fig. 8. (a) How the probe leaves behind a pad stub. Also shown are equivalent circuits of a: (b) probe-pad stub and (c) coplanar probe and stub.

on the properties of the substrate (its permittivity and conductivity). The mutual inductance and capacitance are determined by the angle of the probe to the pad. The values of the probe's elements also depend on the probe's construction. All element values are affected by the size of the probe pad. When the pad area increases, C_{st} and G_{st} increase, while L_{st} and R_{st} decrease. Of the stub's parasitics, C_{st} dominates. Ideally, the stub capacitance on the alumina impedance standard substrate (ISS) should be the same as the stub capacitance on the wafer. A pad with a lower dielectric constant pad can be physically large, just as a lower dielectric constant results in a wider microstrip line (for the same capacitance). The pad's impedance on an Si wafer is complex because, unlike GaAs, a pure reactance correction is not enough. To quantify these concepts, put the same probe-pad pattern on both alumina and the wafer and then measure the shunt capacitances and compare.

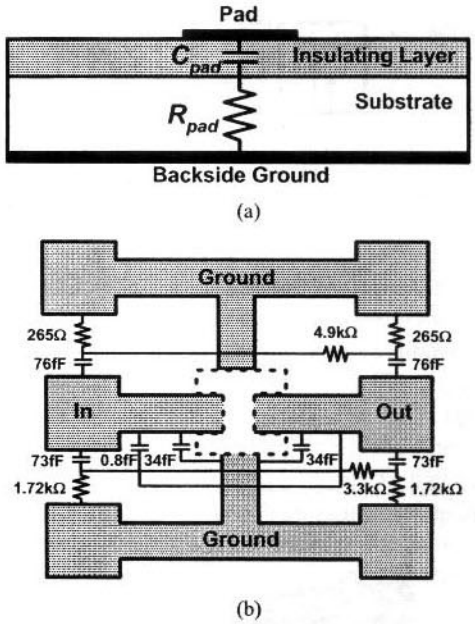

Fig. 9. Probe pads and interconnecting lines leading to the DUT (dotted line). (a) Vertical view of a probe pad on a conductive substrate. (b) Typical parasitics of the probe pads and interconnects on a Si substrate.

Understanding the probe pads and interconnects is key to accurate device modeling. Fig. 9(a) shows a diagram of a typical DUT probe pad and interconnect scheme on silicon. Cross sectioning the wafer, the probe pads rest atop a dielectric insulating layer, either oxide or polymide, to lessen the line's insertion loss. The value of the probe pad's high-Q capacitance $C_{\rm pad}$ is 0.1–0.3 pF, whose exact value depends on the pad's size, dielectric material, and thickness. The resistance $R_{\rm pad}$ is a function of the substrate's resistivity and pad dimensions. At higher frequencies, $C_{\rm pad}$ and $R_{\rm pad}$ become complex functions of frequency. Shown schematically in Fig. 9(b) is a first-order electrical model of the parasitics, good for <3 GHz [19]. The resistor values are determined by the amount of coupling through the substrate, while the capacitance depends on the fringing fields between the pads and interconnects.

For an accurate DUT measurement, the probe pad and interconnecting lines must be dealt with in some way, whether through modeling and extraction, cold-FET measurements, pad parasitic removal, EM modeling, conventional calibration, etc. The first inclination is to use on-wafer calibration standards mounted in place of the DUT. The difficulty is that most IC processes cannot repeatably deposit a precision 50-Ω load. Rather than calibrating out the probe pads and interconnects, it is simpler to either model or deembed them. Step-by-step methods are available for deembedding the probe pads and interconnects [20], [21]. The most common way is to use a set of dummy test structures. Kolding [22] gives an excellent treatment of five methods to deembed the probe pads and interconnects in order of complexity. The number of dummy structures employed increases the measurement accuracy. The methods can be applied to characterizing either passive structures or active devices. Since substrate resistivity and oxide thickness vary with location across the wafer, it is important that the dummy structures be placed near the DUT on the wafer. An additional open structure can be used to specifically study

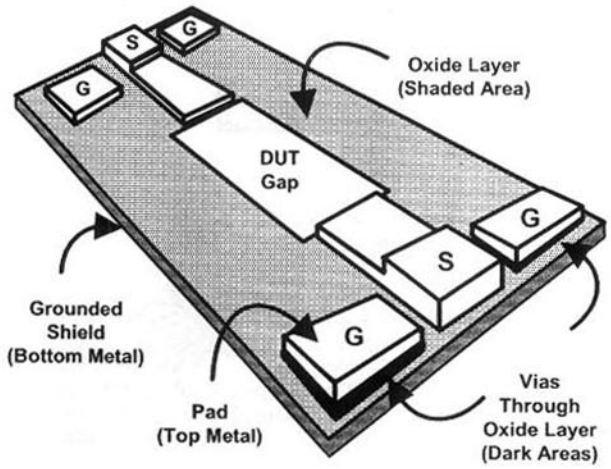

Fig. 10. Surrounding the DUT with a grounded metal shield improves isolation from substrate noise. The probe pads use the top metal with an oxide layer between the top and bottom metal layers. Vias connect the coplanar ground (G) pads through the oxide to the grounded metal shield underneath.

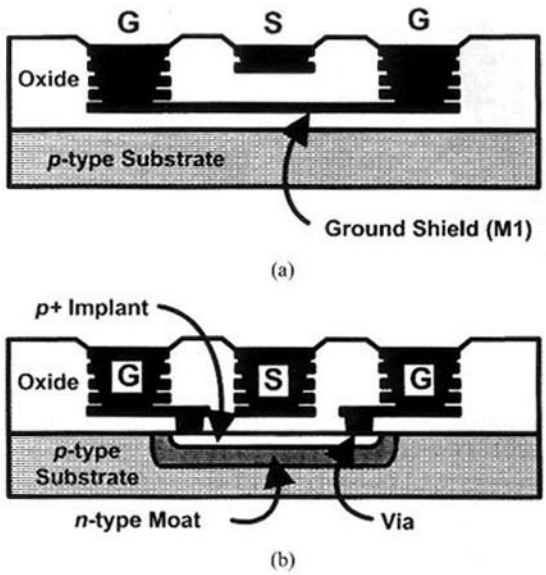

Fig. 11. Two methods of isolating the DUT from the substrate. (a) A metal shield surrounds the DUT similar to Fig. 9. (b) A doped moat in the substrate replaces the metal shield. Both techniques inhibit noise coupling through the substrate to the DUT.

the effects of leakage through the substrate [23]. The structure has a split ground where the RF input and output are spread far apart to more easily quantify isolation [24].

When the input impedance of a device is large (such as with small-periphery FETs), the probe pads become a significant source of noise [25]. In general, the probe pad's noise contribution grows as the device shrinks, with the pad eventually dominating the measurement. As shown in Fig. 9(a), the probe pad capacitively couples through the oxide layer to the substrate. Current traveling laterally through the substrate generates noise that couples to probe pads on the surface. Probe pads are particularly sensitive to noise on a semiconductive Si substrate. The pads can also pick up substrate thermal noise. In general, pad coupling to the substrate reduces the DUT's gain, increases its noise figure, and degrades its port-to-port isolation.

To combat these detrimental noise effects, start by designing a low-noise probe pad and interconnect scheme. Fig. 10 illustrates a low-noise bond pad and interconnect layout. Afterwards, employ a method of deembedding the probe pad and interconnect noise [26], [27]. A variety of probe pad and interconnect designs are available to lessen the substrate's noise contribution (see Fig. 11). A grounded-metal layer underneath the probe pads surrounds the DUT and shields the probe pads and interconnects from the substrate. The bottom metal layer is grounded. Widening it lessens the inductance in the ground path. Vias through the oxide connect the coplanar ground pads to the shield underneath. By connecting all the coplanar ground pads to the shield, a common ground reference is ensured to all circuit ports. Using all the metal layers under the pads yields better pad-to-pad planarity for coplanar probing. When a metal shield is not available due to a limited number of metal layers, encircling the DUT with a p^+ implant "moat" is another possibility. The moat connects to the ground probe pads on the top surface [28], [29]. Electrically, the moat acts as a small shunt resistance in parallel with the pad-to-substrate capacitance, effectively shorting it out. Of the two approaches, the metal shield is preferable. It has less parasitic capacitance and less resistance in the ground path compared with the moat. A third approach is to completely encircle the DUT with ground vias, building a virtual Faraday cage around it [30]. The ring of vias cuts completely through the substrate to the ground plane on back of the wafer. On the wafer surface, all the vias are connected together with a metal track, encircling the DUT.

When modeling devices with different size peripheries, one set of shielded deembedding structures is enough to deembed all the devices [31]. Otherwise, repeating the same deembedding structures for each size DUT takes up valuable real estate on the wafer. Referring to Fig. 10, size the DUT gap to fit the largest DUT on the wafer. Keeping the pads and interconnect routing the same, scale the gap to fit the DUT. By using this approach, the parasitics of the shielding structure become well defined and fixed. Since they do not scale with the DUT, the same parasitics can be deembedded for all size DUTs.

III. Characterizing a Coplanar Probe

With a well-designed probe, the probe's parasitics are low (permitting wide-band measurements) and the measurement reference plane is easily defined (for easier calibration). This section addresses the first point, where carefully characterizing the probe helps to understand the effect of its parasitics on the measurement. The second point is dealt with in other sections. There are a number of methods to directly characterize a coplanar probe [32]. One way is to visualize the probe as a simple coaxial-to-CPW adapter, employing the vector network analyzer's (VNA) adapter removal feature [33]. Consider one of the two coplanar probes as an adapter and carry out a short–open–load–thru (SOLT) calibration with adapter removal. To begin, perform the short–open–load (SOL) steps of a SOLT calibration on one of the coplanar probes. The other probe then becomes the "adapter" probe. Disconnect the adapter probe and perform the SOL steps at the coaxial

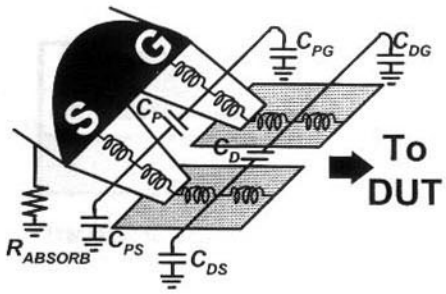

Fig. 12. Equivalent circuit of an S–G coplanar probe contacting the die's probe pads.

connector. Afterwards, reconnect the adapter probe and perform the final thru steps of the SOLT calibration, placing both sets of probes on a substrate thru. Once the SOLT calibration is complete, use both coplanar probes to measure the thru standard again. The test system now considers the adapter probe to be the DUT. Measuring a known short, open or load on the ISS helps quantify and validate the model of the probe.

Fig. 12 shows an equivalent circuit model of a signal–ground (S–G) coplanar probe contacting probe pads [34]. The ground is either on back of the wafer or the wafer chuck. Capacitance $C_{\rm P}$ arises between the signal and ground probe tips, with fringing capacitance $C_{\rm PS}$ and $C_{\rm PG}$ at the probe's outer edges. $C_{\rm PG}$ mostly terminates on the ground probe pad. $C_{\rm PS}$ originates at the signal probe edge and, without any other ground nearby, is smaller than $C_{\rm PG}$ due to the distance to ground. Ideally, the ground probe tip and the ground probe pad are at the same potential to make $C_{\rm PG}$ small (<1 fF). When the ground pad has nearly the same potential as the wafer backside, $C_{\rm DG}$ will be lower than $C_{\rm PG}$. The exact values of the capacitances depend on the properties of the wafer (its thickness and dielectric properties). Since it has one less ground probe than G–S–G, the ground inductance of a S–G coplanar probe is about twice that of a G–S–G probe. In terms of mutual inductance, the missing ground probe has a significant effect on the inductors shown in Fig. 12.

Without adequate vias, the potential of the ground pads will be different from the potential of the ground plane on the back of the wafer. A potential difference in the top and bottom grounds brings about a common-mode current flowing through the probe's ground. To terminate the common-mode current, an RF absorber ($R_{\rm ABSORB}$) is applied to the bottom of the probe. The absorber dampens traveling waves produced by common-mode current from flowing through the probe. These traveling waves move back through the probe toward the test system.

IV. Probe Configurations

The most popular coplanar probe configuration is G–S–G. Its principal advantage is in tightly controlling the fields around the signal probe (see Fig. 13). Electric fields from the signal (S) probe terminate on the ground (G) probes on either side, while the magnetic fields between S and G cancel. This balance can lead to a small measurement error when probing an unbalanced load (see Fig. 14). For example, consider a 50-Ω load realized by two 100-Ω resistors in parallel. The mutual inductances M on either side of the signal (S) tip are balanced due to equal current division between the grounds. When measuring an actual DUT, the ground currents are rarely equal. A ground current imbalance leads to parasitics that are different from those deembedded during calibration. Unbalanced currents can also give rise to higher order modes. Ideally, the load used in calibration should emulate the load presented by the DUT. Differences between the DUT load and calibration load currents impact miniscule capacitance and inductance measurements.

Other probe configurations beside G–S–G are available. Another popular probe is the S–G or ground–signal (G–S) probe. One less ground pad reduces the die's overall size, increasing the number of die per wafer. The drawback is that one less ground probe means less shielding, resulting in poor isolation. The transition from coaxial mode to S–G (or slot line) mode launches unwanted modes onto the subminiature coaxial's ground shield. In close proximity to the wafer surface, the coaxial ground shield couples the unwanted modes to

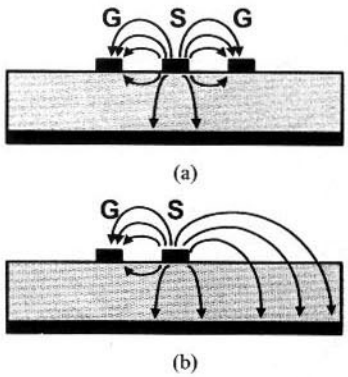

Fig. 13. Electric fields in: (a) G–S–G and (b) G–S probes. (a) Illustrates the balanced electric-field pattern of CPW probe tips on a wafer. (b) Illustrates how the right side of a G–S probe can couple to nearby structures, degrading isolation.

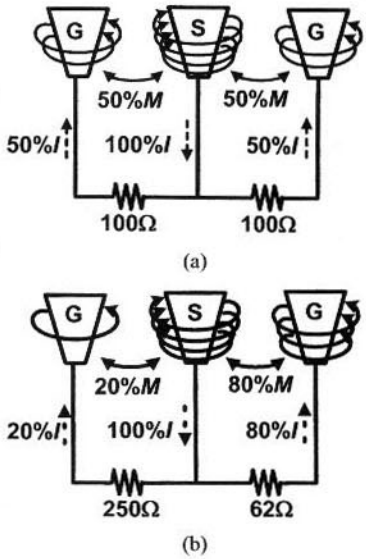

Fig. 14. How the DUT load affects the probe's parasitics. (a) Currents (dotted lines) through a balanced 50-Ω load. The equivalent DUT load in (b) is still 50 Ω, however, the ground currents are unbalanced causing the magnetic fields (solid lines) around one ground probe to be stronger. This changes the mutual and self inductances, causing return-loss error in high-isolation measurements (below 50 dB).

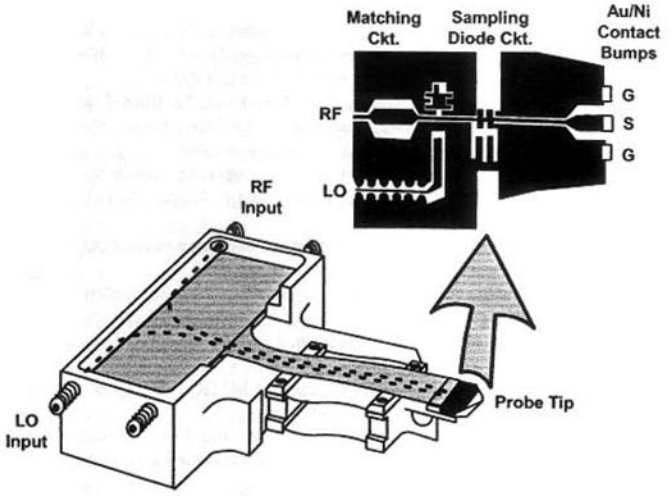

Fig. 15. Construction of a 500-GHz probe. Subminiature coaxial lines (shown as dotted lines) connect 50 GHz external RF to a GaAs IC circuit mounted at the probe tip. An exploded view details the millimeter-wave GaAs IC up-conversion circuit at the tip.

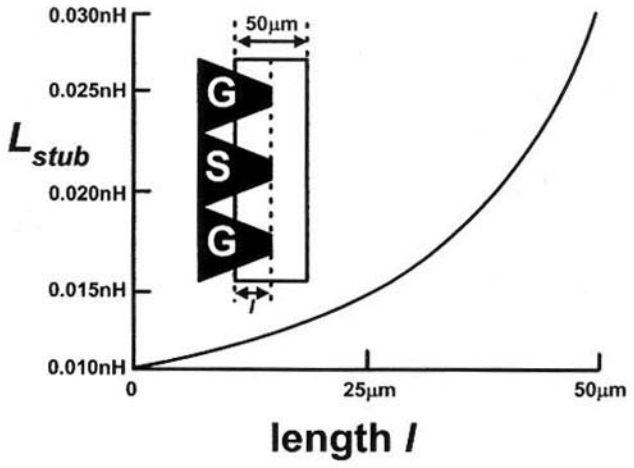

Fig. 16. Impact of skating on a shorting bar deposited on an alumina ISS. As the probe skates a length l, it increases the stub's inductance L_{stub}.

the wafer's ground, impacting the DUT measurement [35]. Comparable to G–S–G probes, signal–ground–signal (S–G–S) probes are popular with differential circuits, yet suffer from crosstalk and poor isolation when used in common-mode circuits. Inductance in the shared ground probe serves as a coupling path between the two signal probes. In general, S–G–S probes are best used below 10 GHz.

In many foundries, on-wafer testing is regularly performed using needle probes, reliable for carrying RF signals up to a few megahertz. Since they are long, needle probes have excessive series inductance (~1 nH/mm) and minor fringing capacitance, limiting their high-frequency ability. Needle probes are constructed of a solid conductor with no corresponding ground shielding. High-frequency signals require a ground path as close as possible to the signal path. Simply making a ground strap connection to the chuck will not suffice as an RF ground. In such cases, coplanar probes are a better solution.

At millimeter-wave frequencies, loss in the cable connecting the test system to the probe tip becomes high. When plotting a return-loss measurement, high loss keeps the measurement trace from reaching the outer edge of the Smith chart. Placing an active device inline is the usual way to overcome system loss. Instead of amplifying a millimeter-wave signal, another solution is to supply the RF at a lower frequency where less insertion loss accumulates. Afterwards, the RF is up-converted at the probe tip to the test frequency. Fig. 15 shows the construction of a 500-GHz bandwidth probe with active tuning elements built into the probe tip [36]. GaAs mixing diodes mounted either $\lambda/4$ or $\lambda/2$ from the tip also enable a wide range of impedances to be presented to the DUT. It is possible to build other active components into the probe tip such as varactor or p-i-n diodes to enable noise or load–pull measurements [37].

V. Calibration and Repeatability

Calibrating with a commercial ISS is the best way to define the measurement reference plane at the probe tips. Made of alumina, the ISS holds standards for calibration methods such as SOLT [38], SOL-reciprocal (SOLR) [39], [40], thru–reflect–line (TRL) [41] and line–reflect–match (LRM) [42]. Employing an ISS can inadvertently highlight the difference in properties between the ISS and wafer. The calibration coefficients entered into the VNA correctly for the pad parasitics on the ISS, but not on the wafer. Since the ISS is made of alumina ($\varepsilon_r = 9.8$), the probe-tip-to-probe-pad parasitics are different from those on either GaAs ($\varepsilon_r = 13.1$) or Si ($\varepsilon_r = 11.9$). In general, an alumina substrate exhibits less capacitance than GaAs or Si due to its permittivity ε_r. The impact ε_r has on the capacitance of the calibration standards is more important than the effect ε_r has on pad capacitances, such as C_{pg} or C_{ps} (see Fig. 12). In addition to ε_r, the pad parasitics are also affected by the length of the probe-pad stub and the quality of the probe's transitions.

During calibration, the probe contacts a slightly different spot on the pad each time it touches down, resulting in repeatability error. Random variation in the probe contact point impacts the measurement through changing contact resistance and pad inductance [43]. A common mistake is to readjust the probes when moving from one calibration standard or DUT to the other. Before beginning calibration, set the micropositioners once and do not change their position once calibration has started. Movement of the probes will change the standards' parasitics, in particular its inductance [44]. With coplanar probes, the amount of inductance depends on the amount the probe overlaps with the standard (see Fig. 16). In general, the pad's series inductance changes by ± 0.15 pH for each μm of probe displacement.

Understanding measurement variation is especially important when measuring quantities on the order of femtofarads or picohenrys. The variation in touchdown characteristics can be statistically averaged to find the true on-wafer measurement [45]. To illustrate, consider the case of making an accurate S_{11} measurement of a die on a wafer. To determine the repeatability of the S_{11} measurement, first calculate the mean difference

$$\Delta S_{11\text{mean}} = \frac{\sum_{i=1}^{n} \frac{\left|S_{11}^{\text{baseline}} - S_{11}^{\text{measured},\,i}\right|}{\left|S_{11}^{\text{baseline}}\right|}}{n} \tag{1}$$

where S_{11}^{measured} is the measured complex return loss, n is the number of repeated touchdowns on the same set of die pads, and $S_{11\text{baseline}}$ is the average S_{11} measurement made of similar die on the same wafer. $\Delta S_{11\text{mean}}$ is computed at each frequency point. The same die can be probed ten ($n = 10$), 20 ($n = 20$), or 30 ($n = 30$) times. Computing $\Delta S_{11\text{mean}}$ for each value of n, the rms value K_{rms} can be found as follows:

$$K_{\text{rms}} = \left[\frac{\sum_{j=1}^{\text{nf}} \left((\Delta S_{11\text{mean},\,a} - \Delta S_{11\text{mean},\,b})_j \right)^2}{\text{nf}} \right]^{1/2} \tag{2}$$

where nf is the number of frequency points. The a and b subsets denote the different $\Delta S_{11\text{mean}}$ datasets. For example, $\Delta S_{11\text{mean},\,a}$ could be the mean return loss for $n = 20$ touchdowns and $\Delta S_{11\text{mean},\,b}$ for $n = 30$ touchdowns. The data will have converged on the actual ΔS_{11} when K_{rms} changes by less than a half an order of magnitude from the previous K_{rms} calculation. In this case, K_{rms} calculations can be for n_a and n_b of either 5 and 10, 10 and 20, or 20 and 30, respectively. Again, when K_{rms} converges, an accurate value of S_{11} has been arrived at.

VI. Summary

The coplanar probe is a popular instrument for transitioning an RF signal from the test system to the wafer. This tutorial highlights specific issues to consider when using coplanar probes, related to their construction, characterization, selection, calibration, and repeatability.

References

[1] K. Mayaram, D. Lee, S. Moinian, D. Rich, and J. Roychowdhury, "Computer-aided circuit analysis tools for RFIC simulation: Algorithms, features, and limitations," *IEEE Trans. Circuits and Syst. II*, vol. 47, pp. 274–286, Apr. 2000.

[2] J. Carbonero, G. Morin, and B. Cabon, "Comparison between beryllium-copper and Tungsten high frequency air coplanar probes," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2786–2793, Dec. 1995.

[3] S. Liu and G. Boll, "Probe design extends on-wafer testing to 120 GHz," *Microwaves RF*, vol. 32, no. 6, pp. 104–110, 1993.

[4] S. M. J. Liu and G. G. Boll, "A new probe for W-band on-wafer measurements," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 1335–1338.

[5] A. Prabhu and N. Erickson, "A 40 to 50 GHz HEMT test fixture," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1995, pp. 427–429.

[6] G. Dalman, "New waveguide-to-coplanar waveguide transition for centimeter and millimeter wave applications," *Electron. Lett.*, vol. 26, no. 13, pp. 830–831, 1990.

[7] G. Ponchak and R. Simons, "A new rectangular waveguide to coplanar waveguide transition," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1990, pp. 491–492.

[8] E. M. Godshalk, "A V-band wafer probe using ridge-trough waveguide," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 2218–2228, Dec. 1991.

[9] ——, "A W-band wafer probe," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 171–174.

[10] ——, "A V-band wafer probe using ridge-trough waveguide," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1991, pp. 1129–1132.

[11] R. L. Eisenhart, "A better microstrip connector," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1978, pp. 318–320.

[12] M. Yu, R. Vahldieck, and J. Huang, "Comparing coaxial launcher and wafer probe excitation for 10 mil conductor backed CPW with Via holes and airbridges," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 705–708.

[13] R. Y. Yu, J. Pusl, Y. Konishi, M. Case, M. Kamegawa, and M. Rodwell, "A time-domain millimeter-wave vector network analyzer," *IEEE Microwave Guided Wave Lett.*, vol. 2, pp. 319–321, Aug. 1992.

[14] N. Muthukrishnan, S. M. Riad, and A. Elshabini-Riad, "A thick-film coplanar probe for time domain measurements," *IEEE Trans. Comp. Hybrids, Manufact. Technol.*, vol. 12, pp. 297–302, June 1989.

[15] G. Ghione and C. Naldi, "Analytical formulas for coplanar lines in hybrid and monolithic MICs," *Electron. Lett.*, vol. 20, no. 4, pp. 179–181, 1984.

[16] "On-wafer vector network analyzer calibration and measurements," Cascade Microtech, Beaverton, OR, Applicat. Note, 1998.

[17] G. Carchon, B. Nauwelaers, W. De Raedt, D. Schreurs, and S. Vandenberghe, "Characterising differences between measurement and calibration wafer in probe-tip calibrations," *Electron. Lett.*, vol. 35, no. 13, pp. 1087–1088, 1999.

[18] K. Jones, "Verify wafer-probe reference planes for MMIC testing," *Microwaves RF*, vol. 27, no. 4, pp. 75–91, 1988.

[19] N. Camilleri, J. Kirchgessner, J. Costa, D. Ngo, and D. Lovelace, "Bonding pad models for silicon VLSI technologies and their effects on the noise figure of RF NPNs," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.*, 1994, pp. 225–228.

[20] H. Cho and D. Burk, "A three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, pp. 1371–1375, June 1991.

[21] E. Vandamme, D. Schreurs, and C. Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer test structures," *IEEE Trans. Electron Devices*, vol. 48, pp. 737–742, Apr. 2001.

[22] T. E. Kolding, "On-wafer calibration techniques for gigahertz CMOS measurements," in *IEEE Int. Microelectronic Test Structures Conf.*, vol. 12, 1999, pp. 105–110.

[23] ——, "Impact of test-fixture forward coupling on on-wafer silicon device measurements," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 73–74, Feb. 2000.

[24] C.-H. Kim, C. S. Kim, H. K. Yu, and K. S. Nam, "An isolated-open pattern to de-embed pad parasitics," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 96–98, Feb. 1998.

[25] M. Deen and C. Chen, "The impact of noise parameter de-embedding on the high-frequency noise modeling of MOSFET's," in *IEEE Int. Microelectronic Test Structures Conf.*, vol. 12, 1999, pp. 34–39.

[26] C. E. Biber, M. L. Schmatz, T. Morf, U. Lott, E. Morifuji, and W. Bachtold, "Technology independent degradation of minimum noise figure due to pad parasitics," in *IEEE MTT-S Microwave Symp. Dig.*, 1998, pp. 145–148.

[27] C. Y. Su, L. P. Chen, S. J. Chang, G. W. Huang, Y. P. Ho, B. M. Tseng, D. C. Lin, H. Y. Lee, J. F. Kuan, Y. M. Deng, C. L. Chen, L. Y. Leu, K. A. Wen, and C. Y. Chang, "Effect of coplanar probe pad design on noise figures of 0.35 μm MOSFETs," *Electron. Lett.*, vol. 36, no. 15, pp. 1280–1281, 2000.

[28] J. Colvin and S. Bhatia, "A bond-pad structure for reducing effects of substrate resistance on LNA performance in a silicon bipolar technology," in *IEEE Bipolar Circuits and Technology Meeting*, 1998, pp. 109–112.

[29] C. Biber, T. Morf, H. Benedickter, U. Lott, and W. Bachtold, "Microwave frequency measurements and modeling of MOSFET's on low resistivity silicon substrates," in *IEEE Int. Microelectronic Test Structures Conf.*, vol. 9, 1996, pp. 211–215.

[30] J. H. Wu, J. Scholvin, J. A. del Alamo, and K. A. Jenkins, "A Faraday cage isolation structure for substrate crosstalk suppression," *IEEE Microwave Wireless Comp. Lett.*, vol. 11, pp. 410–412, Oct. 2001.

[31] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1039–1044, June 2001.

[32] S. A. Wartenberg, *RF Measurements of Die and Packages*. Boston, MA: Artech House, 2002, pp. 60–61.

[33] "Measuring noninsertable devices," Hewlett-Packard, Santa Rosa, CA, Applicat. Note 8510–13, 1991.

[34] "A guide to better vector network analyzer calibrations for probe-tip measurements," Cascade Microtech, Beaverton, OR, Tech. Brief, 1998.

[35] E. Godshalk and G. Sundberg, "Modeling ground signal probe invasiveness and its effect on extracted inductor Q," in *59th Automatic RF Conf. Technical Dig.*, 2002, pp. 62–70.

[36] M. S. Shakouri, A. Black, B. A. Auld, and D. M. Bloom, "500 GHz GaAs MMIC sampling wafer probe," *Electron. Lett.*, vol. 29, no. 6, pp. 557–558, 1993.

[37] G. Rabjohn and R. Surridge, "Tunable microwave coplanar probes," in *IEEE GaAs IC Symp. Dig.*, 1988, pp. 213–216.

[38] L. Glasser, "An analysis of microwave de-embedding errors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 379–380, May 1978.
[39] S. Basu and L. Hayden, "An SOLR calibration for accurate measurement of orthogonal on-wafer DUTs," Cascade Microtech, Beaverton, OR, Applicat. Note, 1995.
[40] A. Ferrero and U. Pisani, "Two-port network analyzer calibration using an unknown thru," *IEEE Microwave Guided Wave Lett.*, vol. 2, pp. 505–507, Dec. 1992.
[41] C. Engen and C. Hoer, "Thru–reflect–line: An improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Trans. Microwave Theory Tech.*, vol. 27, pp. 987–993, Dec. 1979.
[42] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM calibrations with automatic determination of load inductance," Cascade Microtech, Beaverton, OR, Applicat. Note, 1995.
[43] E. M. Godshalk, J. Burr, and J. Williams, "An air coplanar wafer probe," in *43rd Automatic RF Conf. Technical Dig.*, 1994, pp. 70–75.
[44] E. Strid, "Planar impedance standards and accuracy considerations in vector network analysis," Cascade Microtech, Beaverton, OR, Applicat. Note, 1986.
[45] C. L. Hammond and K. L. Virga, "Network analyzer calibration methods for high-density packaging characterization and validation of simulation models," in *IEEE Electronic Components Technology Conf.*, 2000, pp. 519–525.

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