THz Indium Phosphide Bipolar Transistor Technology

M. J. W. Rodwell[1], J. Rode[1], H.W. Chiang[1], P. Choudhary[1], T. Reed[1], E. Bloch[1], S. Danesgar[1],
H-C Park[1], A. C. Gossard[2], B. J. Thibeault[1], W. Mitchell[1],
M. Urteaga[3], Z. Griffith[3], J. Hacker[3], M. Seo[3], B. Brar[3]

Department of Electrical Engineering[1] and of Materials[2],
University of California, Santa Barbara, CA 93105
Teledyne Scientific Company[3], Thousand Oaks, CA.

Abstract — **Scaling laws and limits of THz indium Phosphide heterojunction bipolar transistors (HBTs) are presented. The primary limits to scaling through the 32 nm / 3 THz node are the resistivity, penetration depth, and current-carrying capability of the emitter and base contacts. A processes flow with refractory dry-etch emitter and base contacts is presented. Beyond the 32 nm node, degenerate injection in the emitter-base junction limits transconductance and impedes scaling. At the 32 nm node, bandwidths will be sufficient for 1.4 THz transmitters and receivers.**

Index Terms — wireless ICs, bipolar transistors, THz technology.

I. Introduction

Emerging applications for high frequency electronics include wireless systems at higher mm-wave (100-300 GHz) and far-infrared (0.3-3 THz) frequencies. Though rain attenuation limits terrestrial applications to ~ 1 km range, available spectral bandwidths are large, providing large capacity for high-rate communications links. The wavelengths are short, which permits narrow and tightly-collimated beams to be radiated from even small phased arrays. This will enable high-resolution imaging for automotive and security applications, and dense spatial packing of signal beams for high-capacity communications networks. Bands of relatively low attenuation, for communications, include those near 140, 220, and 340 GHz. Bands of moderately higher attenuation, but with shorter wavelengths useful for high-resolution imaging, including those at 400, 670, and 1030 GHz.

ICs operating beyond 1 THz will soon be feasible. There is intense competition among technologies for these applications, with InP HBTs [1, 2] and HEMTs [3], SiGe bipolar [4], CMOS [5,6], and GaN power HEMTs [7] all exhibiting cutoff frequencies between 300-1200 GHz. Despite the rapid progress in CMOS and SiGe bipolar technologies, cutoff frequencies and breakdown voltages of InP HBTs remain 2:1 to 3:1 larger, allowing larger operating frequencies and greater output power.

A major advantage of InP HBT lies in its prospects for further improvement by scaling. Unlike MOSFETs, where geometric scaling of gate lengths for increased bandwidth is compromised once tunneling prevents proportional reduction of the gate oxide thickness, the primary limits to HBT scaling are difficulties in fabrication, in the formation of shallow yet low-resistivity contacts, in high-current-density-operation, and in the removal of heat. With present InP HBTs showing 1.1 THz $f_{\max}$ at the 128 nm node, there are no obviously insurmountable scaling challenges through the 32nm /3 THz generation.

Parameter	scaling law	Gen. 4 (128 nm)	Gen 5 (64 nm)	Gen 6 (32 nm)
MS-DFF speed	γ^1	330 GHz	480 GHz	660 GHz
Amplifier frequency	γ^1	660 GHz	1.0 THz	1.4 THz
Emitter Width	$1/\gamma^2$	128 nm	64 nm	32 nm
Resistivity	$1/\gamma^2$	4 Ω-µm^2	2 Ω-µm^2	1 Ω-µm^2
Base Thickness	$1/\gamma^{1/2}$	212 Å	180 Å	180 Å
Contact width	$1/\gamma^2$	120 nm	60 nm	30 nm
Doping	γ^0	7 10^{19} /cm^2	7 10^{19} /cm^2	7 10^{19} /cm^2
Sheet resistance	$\gamma^{1/2}$	708 Ω	830 Ω	990 Ω
Contact ρ	$1/\gamma^2$	5 Ω-µm^2	2.5 Ω-µm^2	1.25 Ω-µm^2
Collector Width	$1/\gamma^2$	360 nm	180 nm	90 nm
Thickness	$1/\gamma$	75 nm	53 nm	37.5 nm
Current Density	γ^2	18 mA/µm^2	36 mA/µm^2	72 mA/µm^2
$A_{collector}/A_{emitter}$	γ^0	2.9	2.8	2.8
f_τ	γ^1	730 GHz	1.0 THz	1.4 THz
$f_{\max}$	γ^1	1.30 THz	2.0 THz	2.8 THz
$V_{BR,CEO}$		3.3 V	2.75 V	?
I_E / L_E	γ^0	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm

Table 1: HBT scaling laws and InP HBT scaling roadmap.

For mm-wave power amplification, InP HBTs are competitive with GaN HEMTs. For InP HBTs, demonstrated $f_\tau \cdot V_{br}$ products [1] are 1.5-2 $\text{THz} \cdot \text{V}$, while the high f_τ and $f_{\max}$ provide high gain and high efficiency. InP HBT power amplifiers have demonstrated 0.50 W/mm power density at 220 GHz [8], as compared to 1.7 W/mm at 94 GHz with GaN HEMTs [9].

We review HBT scaling laws, identifying key challenges faced presently in scaling, and anticipating difficulties in scaling beyond the 32 nm nodes. A THz

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HBT process technology with refractory high-current contacts will be described, and recent IC results presented.

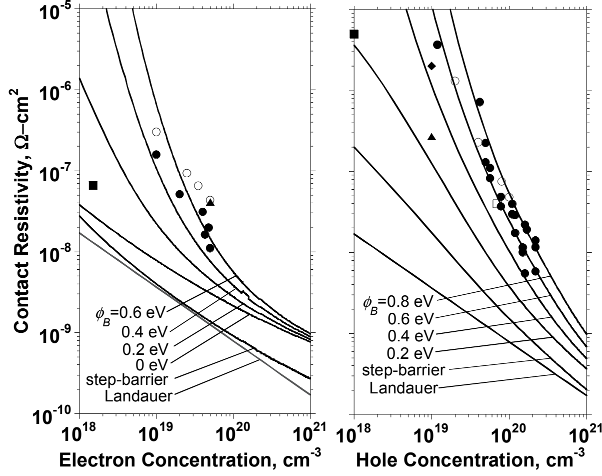

Figure 1: Calculated dependence (represented by lines) of contact resistivities (ρ_c) on bulk electron/hole concentration and Schottky barrier height for (a) n-InGaAs and (b) p-InGaAs. Experimental data from the literature is shown for comparison.

HBT SCALING

First consider HBT scaling laws [10] (Table 1). To increase bandwidth $\gamma:1$, the collector is thinned 1: γ, the base thinned ~1: $\gamma^{1/2}$, and the junction areas reduced 1: γ^2 to reduce transit times and capacitances in the correct proportion. The current density increases $\gamma^2:1$, as enabled by the Kirk effect in the thinned collector; this increased current density is required to reduce $C\Delta V/I$ charging times. All metal-semiconductor contact resistivities must be reduced 1: γ^2 to maintain constant the device parasitic resistances (R_{bb}, R_{ex}). Finally, to maintain nearly constant junction temperature with scaling, the 1: γ^2 reduction in junction area must be obtained by a 1: γ^2 reduction in junction widths while maintaining constant junction (stripe) lengths. Transconductance and DC current per unit emitter length thus remains constant with scaling.

Several effects will modify scaling trends at nodes beyond 32 nm. The laws ignore fringing capacitance in the collector-base junction, of order $\varepsilon_r\varepsilon_0$ ~0.2 fF per μm of emitter length. This is significant in very narrow junctions, and ultimately prevents C_{cb} reduction by width scaling. 1-D current flow in the collector depletion region is assumed. Scaling forces more rapid reductions in the emitter width than in the collector thickness, and for highly scaled devices the collector current spreads laterally under the base contacts. The laws thus underestimate the maximum emitter current density and overestimate the junction self-heating.

Degenerate electron injection is a serious scaling limit. At ~15 mA/μm^2 current density, the Fermi level in the emitter-base junction aligns with the peak of the InP/InGaAs conduction-band barrier, and the injected current then no longer varies exponentially with bias [11]. Transconductance and f_τ are reduced. For strong forward bias, the current varies as the square of voltage, $J_E \cong q^3 m^*(V_{be}-\phi)^2/4\pi^2\hbar^3$, where ϕ is the bias at which injection becomes degenerate. The effect is significant at and beyond the 32 nm node. One extreme solution is to partition the overall emitter area of length L and width W into an array of smaller, electrically-isolated square areas of width and length δl, forming an HBT whose emitter-base junction is an array of 1-D conductors. Degenerate injection then instead introduces a constant series emitter resistance per unit area of $(\pi\hbar/q^2)(\delta l)^2$, e.g. $0.3\,\Omega-\mu\text{m}^2$ for δl=5 nm. A wide-gap emitter of increased m^* is a more immediate solution.

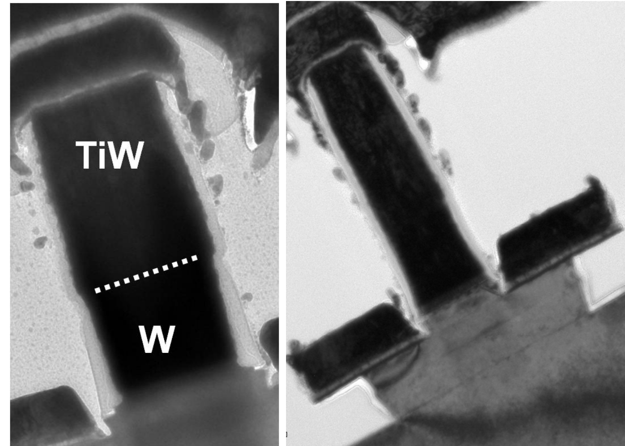

Figure 2: Left: 200 nm Emitter-base junction with Mo contact and dry-etched W/TiW emitter contact via. Right: Complete HBT at 130 nm emitter junction width.

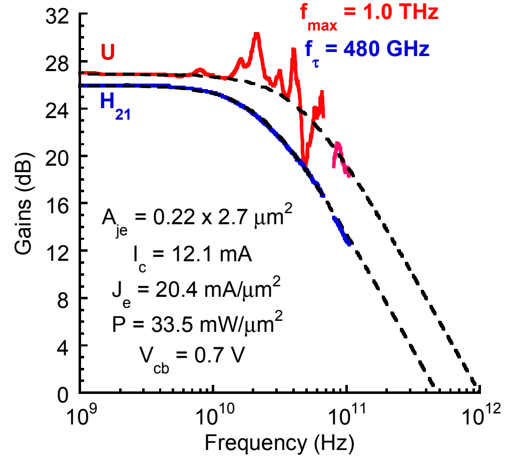

Figure 3: Measured RF Gains of an InP HBT in the refractory W/TiW emitter technology.

REFRACTORY-CONTACT THZ HBT PROCESS

The above laws define the fabrication process. Contact resistivities must be very low, and current densities must be very high. The emitter contact must be stable while operating at very high current densities. The emitter and base contacts must be must be made to very thin

semiconductor layers, and must not penetrate more than ~1 nm into the semiconductor under bias or thermal stress.

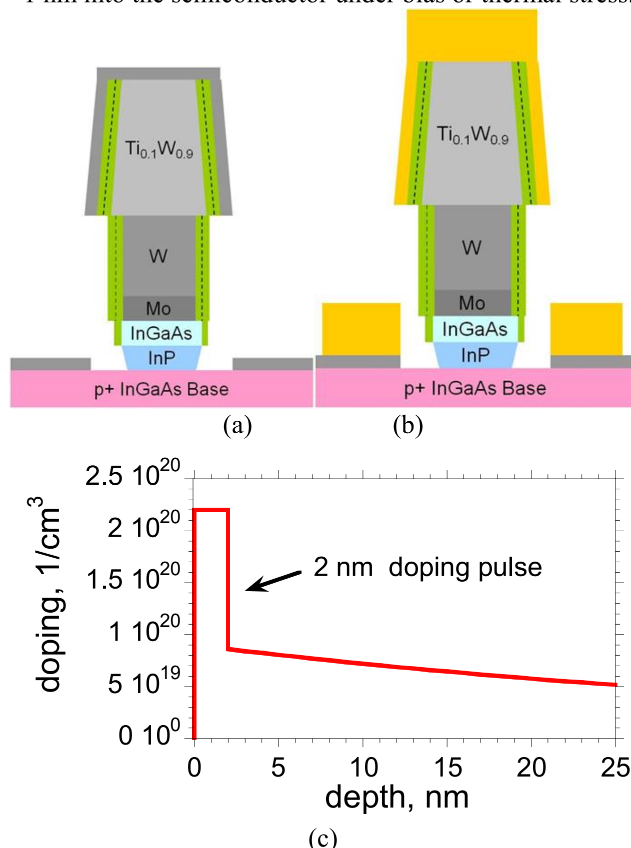

Figure 4: Refractory base metal process. (a): A thin refractory base layer is blanket-evaporated to form the contact. (b): a subsequent thick Ti/Au metal liftoff then provides low metal sheet resistivity along the length of the base stripe. Minimal penetration of the base contact into the semiconductor permits use of a surface doping pulse (c) to reduce contact resistivity.

We have not had success in the formation of 100-nm-width emitters by dry-etching. Instead, the emitter-base junctions are defined by a selective wet etch, and lateral undercutting of the narrow emitter is kept small by using thin (10-20 nm) InP emitter and InGaAs cap layers. The emitter contact, which must operate at 40 mA/μm^2 at the 64 nm node, will be to a cap layer only 5-10 nm thick. For base contacts, we have previously used Pt/Ti/Pt/Au, which reacts and penetrates ~ 5 nm into the InGaAs base. This impairs scaling base thicknesses below 20-25 nm.

Refractory contacts to InGaAs are thus key features of scalable THz HBT processes. Baraskar *et al* [12] (Figure 1) investigated refractory contacts to InGaAs and InAs. To avoid surface contaminants and oxides, *in-situ* contacts were formed by transferring the semiconductor in high vacuum between the growth chamber and an E-beam evaporator. For N-InGaAs, measured contact resistivity is ~2.3:1 higher than theory, in turn only ~4:1 than the $\rho_c = (\hbar / q)^2 (8\pi / 3n)^{2/3}$ Landauer limit of 100% interface quantum transmission probability. These resistivities are sufficient for the 32 nm node.

In-situ emitter contacts are incorporated into an HBT process flow by depositing Mo contact metal immediately after wafer growth. For the base contact, careful surface cleaning [13] can provide *ex-situ* contract resistivities close to those of Figure 1. The emitter Ohmic contact and its post (via) operate at high current densities, and may fail by electromigration; refractory metals are desirable. In our HBT process [2], the emitter contact and via are formed by blanket Mo deposition on the InGaAs emitter cap, and sputter deposition of W and TiW. The via is defined by dry-etching the W/TiW; differences in Ti and TiW sidewall etch rates produce a tapered metal profile. Combined with dielectric sidewalls, this facilitates base contact liftoff.

In the HBTs of Figure 2 and Figure 3, the base contact metals are Pd or Pt, and penetrate ~5 nm into the base. This renders difficult further scaling of both base thickness and the base contact resistivity. Addressing this limitation, Rode and Chiang are developing a refractory base contact process. In this process (Figure 4), after surface cleaning similar to [13], a thin refractory base contact is first blanket-deposited on the clean base surface, avoiding exposure to photoresist and associated surface contamination. Because this thin layer has high sheet resistivity, thick Ti/Au metal is subsequently deposited by liftoff. FIB/TEM images indicate that the thickness of the base under the contact is ~1-2 nm less than that under the emitter, likely as a consequence of surface etching during cleaning.

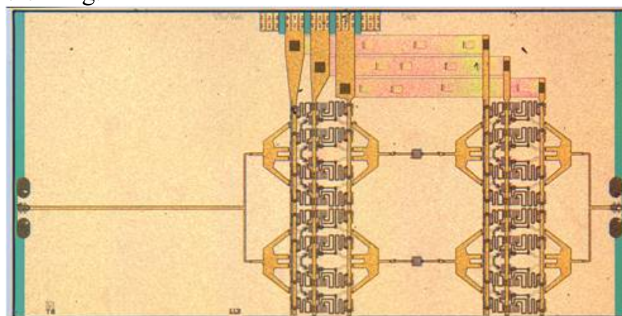

Figure 5: Photomicrograph of a 90 mW, 220 GHz power amplifier in Teledyne's 256 nm InP HBT technology.

Precision in depth control for refractory base contacts permits modified base doping profiles for reduced base contact resistivities. Increased base doping concentration decreases the contact resistivity, and (Figure 1) surface dopings of $\sim 2 \cdot 10^{20}\ /\mathrm{cm}^3$ are desirable. Yet DC current gain in the Auger recombination limit varies as $\beta \propto (N_A T_B)^{-2}$ where N_A is the doping and T_b the base thickness. Experimentally, we observe a more rapid degradation in β with increased doping than is characteristic of Auger recombination, and β<10 would be expected for base doping of $2 \cdot 10^{20}\ /\mathrm{cm}^3$ if present over the full base thickness. High base surface doping and high current gain can be obtained by heavily doping only the upper 2-4 nm of the base layer (Figure 4); analysis (V. Jain, unpublished), by integration of the Auger

recombination rate over the base thickness, suggests that the surface doping spike will not significantly degrade β.

IC RESULTS.

ICs demonstrated in the 256 nm and 128 nm HBT processes [1], include 570 GHz (fundamental) VCOs [14], 300 GHz phase-locked loops [15], 630 GHz transmitter exciter ICs [16], 330 GHz dynamic frequency dividers [17], 50 GS/s sample-hold ICs [18], and 220 GHz power amplifiers with 90 mW output power [19] . These and other IC results will be reported, as will general considerations in >100 GHz IC design.

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