Sub-300 nm InGaAs/InP Type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz f_{max} and 416 GHz f_τ

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***Abstract*— We report InP/InGaAs/InP double heterojunction bipolar transistors (DHBT) fabricated using a simple mesa structure. The devices employ a 30 nm highly doped InGaAs base and a 150 nm InP collector containing an InGaAs/InAlAs superlattice grade. These devices exhibit a maximum f_{max} = 755 GHz with a 416 GHz f_τ. This is the highest f_{max} reported for a mesa HBT. Through the use of i-line lithography, the emitter junctions have been scaled from 500-600 nm down to 250-300 nm – all while maintaining similar collector to emitter area ratios. Because of the subsequent reduction to the base spreading resistance underneath the emitter $R_{b,spread}$ and increased radial heat flow from the narrower junction, significant increases to f_{max} and reductions in device thermal resistance θ_{JA} are expected and observed. The HBT current gain $\beta \approx$ 24-35, BV$_{ceo}$ = 4.60 V, BV$_{cbo}$ = 5.34 V, and the devices operate up to 20 mW/μm^2 before self-heating is observed to affect the DC characteristics.**

***Index Terms*—InP heterojunction bipolar transistor**

I. Introduction

FROM geometric scaling theory [1], [2], the key HBT scaling challenges for balanced increases to f_τ, f_{max}, and digital logic speed are: making narrower emitter and collector junctions, and reducing the emitter and base Ohmic contact resistivity, while being able to operate the device at higher current densities in the limit expected by the Kirk effect $J_{max} \propto T_c^{-2}$. At the 250 nm emitter node, the scaling requisites include an emitter and base $\rho_{c,e}$ = 9 $\Omega \cdot \mu$m^2 and $\rho_{c,b}$ = 10 $\Omega \cdot \mu$m^2, a collector to emitter area ratio A_c/A_e = 2.4, and a J_{max} = 9 mA/μm^2, where a 106 nm thick collector (T_c) is specified. There is an alternative to thinning the collector as a means of increasing the maximum operating J_e before the onset of the Kirk effect. This is an advantageous strategy for digital latch design, as the major delay $\tau = \Delta V_{logic} \cdot C_{cb}/I_c \propto 1/J_e$ – whereas the unity current gain f_τ and maximum osciallation frequency f_{max} are more strongly dependent on $\tau_b \propto T_b^2$ and $\tau_c \propto T_c$, and their delays are secondary amongst digital gate delays.

For the InP type-I DHBTs designed at UCSB, a superlattice InGaAs/InAlAs grade is used to remove the conduction band discontinuity between In$_{0.53}$Ga$_{0.47}$As and InP, in combination with an InGaAs setback, and an InP pulse doping $N_\delta T_\delta$ [3] to establish a quasi-field across the graded region. If this associated dipole is too weak, the electric field will reverse across the grade prematurely and inhibit current flow across the collector at low J_e – or if too strong, the maximum J_e will increase, but severe collector depletion collapse will result at low values of V_{cb}, significantly increasing C_{cb} for the HBT biases used in differential digital logic. After closer examination and better understanding of existing UCSB HBT designs for use in digital logic circuits, it was concluded that the pulse doping $N_\delta T_\delta$ could be increased – subsequently preventing the onset of current blocking at higher J_e operation for a given V_{cb}, with acceptable increases to C_{cb}/A_{jc} (fF/μm^2) and reductions to the breakdown voltages BV$_{ceo}$, and BV$_{cbo}$. The resulting HBT design employs the same T_c, but permits smaller devices (with lower C_{cb}/I_c ratio at J_{max}) to be utilized for a given latch design – resulting in an increased maximum toggle rate for the circuit. Note: this design strategy requires the emitter Ohmic contact resistance ($\Omega \cdot \mu$m^2) be reduced to keep the parasitic voltage drop across the emitter resistance of the differential pair $\Delta V_{parasitic} = I_e \cdot R_{ex} \cong J_e \cdot \rho_{ex}$ unchanged.

At the time of this manuscript, state-of-the-art InP HBT results include InGaAs-collector InP-SHBTs utilizing a 55 nm thick collector, 12.5 nm base demonstrating 765 GHz f_τ [4], as well as Type-II InP-DHBTs (GaAsSb base, InP collector) employing a 150 nm collector, 15 nm base demonstrating 384 GHz f_τ and 262 f_{max} [5]. Prior to this work, the highest reported f_{max} for an InP SHBT and DHBT were 687 GHz (w/ 215 GHz f_τ) [6] and 650 GHz (w/420 GHz f_τ) [7], respectively. An additional point – unlike many previously reported InP SHBTs and DHBTs, the high power density operation associated with the devices here permits the HBTs to be biased simultaneously at high bias voltages and high current densities J_e; an attribute as important as the breakdown voltage in determining the useful voltage capability of a transistor technology [2].

TABLE I

InP DHBT EPITAXIAL LAYER STRUCTURE

Thickness,nm	Material	Doping, cm^{-3}	Description
5	$In_{0.85}Ga_{0.15}As$	$5 \cdot 10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	$4 \cdot 10^{19}$: Si	Cap grading
20	$In_{0.53}Ga_{0.47}As$	$4 \cdot 10^{19}$: Si	Emitter cap
80	InP	$3 \cdot 10^{19}$: Si	Emitter cap
10	InP	$8 \cdot 10^{17}$: Si	Emitter
40	InP	$5 \cdot 10^{17}$: Si	Emitter
30	InGaAs	7 - $4{\cdot}10^{19}$: C	Base
15	InGaAs	$3.5 \cdot 10^{16}$: Si	Setback
24	InGaAs/InAlAs	$3.5 \cdot 10^{16}$: Si	B-C grade
3	InP	$3.5 \cdot 10^{18}$: Si	δ - doping
108	InP	$3.5 \cdot 10^{16}$: Si	Collector
5	InP	$1 \cdot 10^{19}$: Si	Subcollector
6.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Subcollector
300	InP	$2 \cdot 10^{19}$: Si	Subcollector
—	InP	Semi-insulating	Substrate

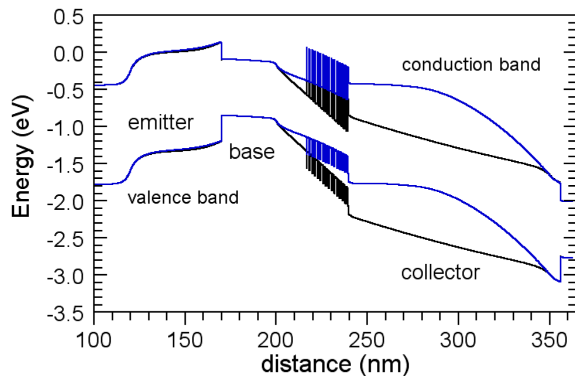


Fig. 1. Simulated energy band diagrams for the 30 nm base, 150 nm collector UCSB type-I InP DHBT at bias V_{cb} = 0.6 V and J_e = 0, 10 mA/μm^2.

II. Design

The epitaxial design was intended to produce devices to be used in 150 GHz current mode logic (CML) and 200 GHz emitter coupled logic (ECL) static frequency divider designs. The base thickness is 30 nm, doped from 7-$4{\cdot}10^{19}$ cm^{-3}:C, producing $\sim$ 45-50 meV of conduction band grading across the base. An average hole mobility $\mu_h \cong 62$ cm^2/V$\cdot$sec is extracted from the measured base sheet resistance.

The full Type-I InP DHBT layer structure is shown in Table I and the associated energy band diagrams [8] of the device at an applied bias of V_{be} = 0.95 V, V_{cb} = 0.6 V for J_e = 0 and 10 mA/μm^2 is shown in fig. 1. For these simulations, the electron velocity in the collector is treated as a two-step profile [9], where from x = 0 to $T_c/2$, υ = $4.5{\cdot}10^7$ cm/sec and from x = $T_c/2$ to T_c, υ = $1.5{\cdot}10^7$ cm/sec. Current spreading is also considered for a 300 nm emitter junction. From [10], it is assumed that the amount of spreading per side of the emitter stripe is $\sim T_c$ = 150 nm – as such, current spreading is treated in the following way across the collector from base to sub-collector: from x = 0 to $T_c/3$ no spreading, from x = $T_c/3$ to $2T_c/3$ 100 nm of total spreading, and from $2T_c/3$ to T_c 200 nm of total spreading.

Compared to previous 150 nm collector UCSB InP DHBT designs [11], the pulse doping $N_\delta \cong 2.5{\cdot}10^{18}$ cm^{-3} ($N_\delta T_\delta \cong 7.5 \cdot 10^{18}$ cm^{-2}) has been increased to $N_\delta \cong 3.5 \cdot 10^{18}$ cm^{-3} ($N_\delta T_\delta \cong 1.05 \cdot 10^{18}$ cm^{-2}) – where the increased quasi-field permits the HBT to operate at higher J_e before the onset of field reversal across the InGaAs/InAlAs grade (Kirk effect for InP type-I DHBTs). The design trade-off however is that collector depletion collapse at the sub-collector side of the collector is more severe at lower V_{cb} due to the reduced electrical field between the dipole and sub-collector. Additionally, the main breakdown mechanism for these devices is tunneling through the setback region [12]. Consequently, the increased potential drop across the setback due to the increased dipole strength will result in small reductions to BV_{ceo}, BV_{cbo}. Keeping in mind the HBT bias conditions within CML and ECL, the increase of C_{cb}/A_{jc} (fF/μm^2) is small and acceptable, as the maximum $J_{e,max} = J_{Kirk}$ has increased $\sim 2\times$, reducing the dominant latch delay τ = $(C_{cb}/I_c) \cdot \Delta V_{logic} \propto 1/J_e$ through the use of smaller devices for a given digital latch design.

This design strategy is affirmed from the Bandprof simulation of the HBT in fig. 1 where $J_e = 10$ mA/μm^2 $= J_{Kirk}$. Electrons entering the collector from the base are accelerated by the $\sim$ 210 meV of potential difference across the conduction band of the setback layer and an additional 31 meV across the grade. At higher simulated values of J_e, the potential difference across the setback changes little; however the field across the grade progressively reverses and significant reductions in the electron velocity in the collector are expected and observed in measurement.

III. Growth and Fabrication

The epitaxial material was grown by IQE Inc. on a 3” semi-insulating InP wafer and the HBTs were fabricated in an all wet-etch, triple mesa process. All physical features of the device were defined by I-line lithography. Figure 2 shows an image of a 250 nm HBT prior to wafer passivation and planarization in benzocyclobutene (BCB) – employed to minimize device surface leakage currents. BCB also provides a low-dielectric-constant spacer (ε_r = 2.7, T_{BCB} = 1.6 μm) between the device probe pads and

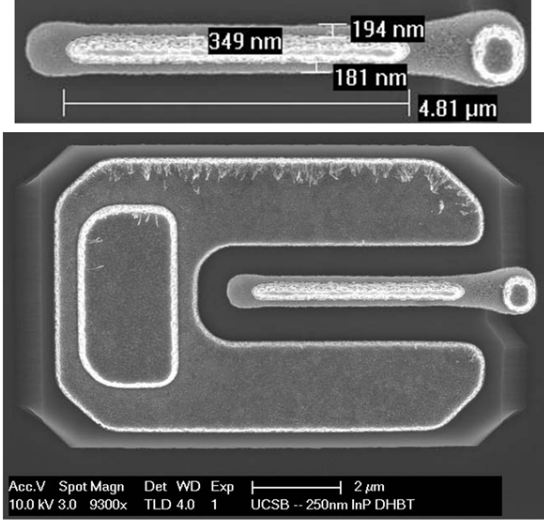


Fig. 2. SEM image of 250 nm UCSB InP DHBT.

the InP substrate to reduce spurious resonances in the RF measurements through substrate mode coupling.

IV. Measurements and Results

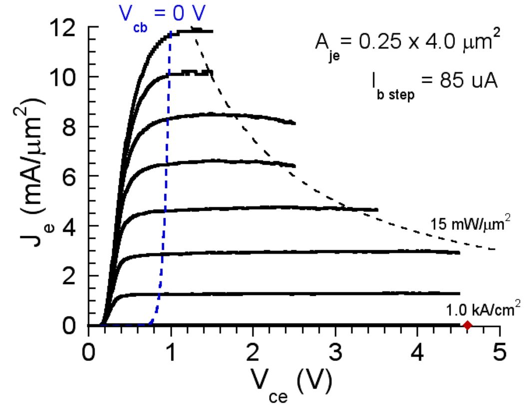
TLM measurements show the base ρ_s = 603 Ω and ρ_c = 6.29 $\Omega \cdot \mu$m^2, collector ρ_s = 12.2 Ω and ρ_c = 6.37 $\Omega \cdot \mu$m^2. From RF parameter extraction, the emitter $\rho_c \cong$ 5.1 $\Omega \cdot \mu$m^2. The DHBTs have a current gain $\beta \cong$ 24-35. The common-emitter BV$_{ceo}$ and common-base BV$_{cbo}$ breakdown voltages at $J_{e,c}$ = 1.0 kA/cm^2 are 4.60 V and 5.34 V respectively, while at $J_{e,c}$ = 10 kA/cm^2, BV$_{ceo}$ = 5.64 V and BV$_{cbo}$ = 6.65 V. The common-emitter I-V and Gummel characteristics for a 250 nm HBT are shown in figs. 3a and 3b respectively.

Thermal resistance θ_{JA} (K/mW) and device junction temperature were determined using the Gummel method from HBTs having 550 nm and 250 nm emitters (both 4 μm in length) across a range of V_{cb} at constant J_e = 6 mA/μm^2. For the 550 nm device the normalized $\theta_{JA} \cong$ 4.4-5.3 K$\cdot\mu$m^2/mW, whereas for the 250 nm device the normalized $\theta_{JA} \cong$ 3.0-3.5 K$\cdot\mu$m^2/mW – a difference of 1.5 : 1. Consequently, self-heating for the 550 nm HBT $\Delta T_{meas} \approx$ 80 K at 15 mW/μm^2 dissipation, but only $\Delta T_{meas} \approx$ 52 K for the 250 nm device.

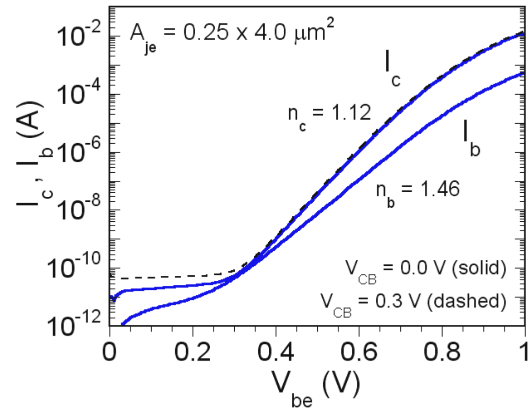
These values of temperature rise are very similar to theoretical prediction. By approximating the heat flow as half-cylindrical at $r < L_E/2$ and as hemispherical at greater distances [13], [14], the junction temperature rise ΔT_{theory} of an isolated HBT on a thick substrate is:

$$\Delta T \cong \frac{P}{\pi K_{InP} L_E} \ln \frac{L_E}{W_E} + \frac{1}{\pi K_{InP} L_E} \quad (1)$$

where W_E and L_E are the width and length of the emitter junction, K_{InP} = 0.68 W/(cm$\cdot$K) is the substrate thermal conductivity and P the dissipated power. Utilizing the same bias conditions for the 550 and 250 nm HBTs as used to determine ΔT_{meas}, the expected temperature rise ΔT_{theory} is 77.8 K and 49.8 K respectively – a difference of $< 5\%$ compared to measurement.



(a) Common-emitter characteristics. $I_{b,step}$ = 85 μA.



(b) Gummel characteristics.

Fig. 3. DC characteristics of 250nm InP DHBT.

DC-67 GHz RF measurements were carried out after performing an off-wafer, probe-tip Line-Reflect-Reflect-Match (LRRM) calibration on an Agilent E8361A PNA. An open and short circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed their associated parasitics from the HBT S-parameter measurements. At a bias associated with peak f_{max}, a maximum 755 GHz f_{max} with a 416 GHz f_τ (fig. 4) was determined from the methods described in [5] – I_c = 6.98 mA and V_{ce} = 1.74 V (V_{cb} = 0.8 V, J_e = 11.6 mA/μm^2, C_{cb}/I_c = 0.37 ps/V, ΔT

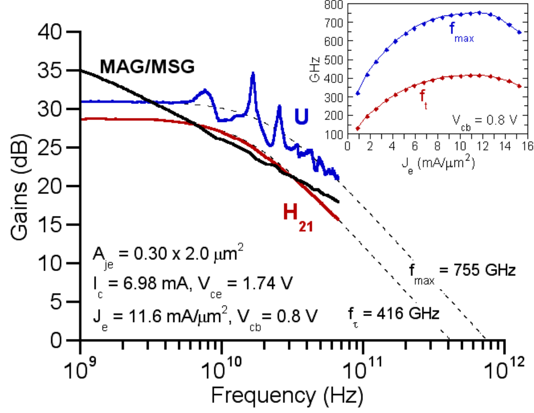


Fig. 4. Measured microwave gains associated with peak f_{max}. A_{je} = 0.30 × 2.0 μm^2, A_{jc} = 0.60 × 3.6 μm^2.

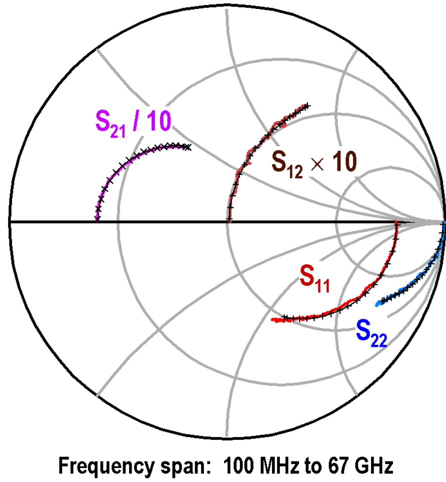


Fig. 5. Measured (fig. 4) and modeled (fig. 6) S-parameters at peak 755 GHz f_{max}.

$\approx$ 75 K). The device has an emitter junction area A_{je} = 0.30 × 2.0 μm^2, 600 nm collector width, and collector to emitter area ratio $A_{jc}/A_{je} \approx 3.6$. For comparison, an HBT having A_{je} = 0.45 × 4.0 μm^2 demonstrated peak f_τ/f_{max} = 420/590 GHz. A small-signal hybrid-π equivalent circuit of the 755 GHz f_{max} HBT at peak bias is shown in fig. 6. The measured S-parameters from fig. 5 show minimal resonances and conform well to the hybrid-π (fig. 6) equivalent circuit for the device. Figure 7 shows the variation of C_{cb} versus operating V_{cb} and J_e for use in 200 GHz emitter coupled (ECL) and 150 GHz current mode logic (CML) digital circuit design.

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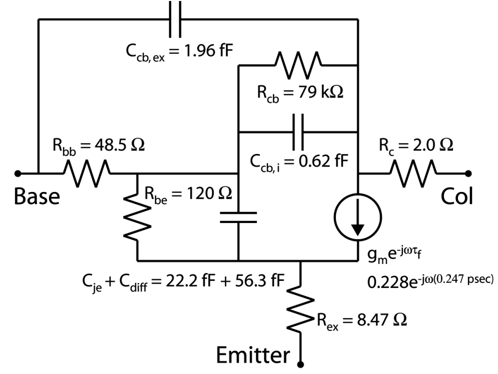

Fig. 6. Hybrid-π equivalent circuit of the HBT at the bias associated with 755 GHz f_{max}.

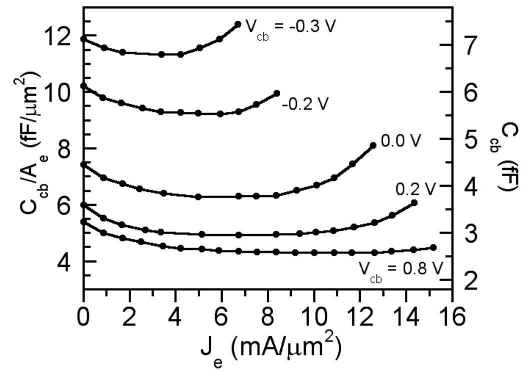

Fig. 7. Variation of C_{cb} versus applied base-collector potential V_{cb} and operating current density J_e. A_{je} = 0.30 × 2.0 μm^2, A_{jc} = 0.60 × 3.6 μm^2.

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