100 GHz Push-Push Oscillator in 90 nm CMOS Technology

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***Abstract*— A 100 GHz fixed-tuned oscillator was designed and fabricated using a 90 nm bulk CMOS process. Push-push mode was chosen to improve the power output. The oscillator exhibits −3 dBm output power at 101 GHz with 27 mW power consumption. The measured SSB phase noise is −85 dBc/Hz at 1 MHz offset. Resonators are implemented with transmission lines to avoid the need of high quality capacitors and inductors.**

I. Introduction

The continuous scaling of CMOS technology has brought transistor operating frequencies well into the millimeter wave frequency range. The cost advantage of CMOS over compound semiconductor technologies and the possibility of integrating low-frequency and digital functions on the same chip is a very tempting prospect. More affordable technology may enable new consumer applications at millimeter wave range where bandwidth is generally more readily available than at lower frequencies. 60 GHz range offers a large unlicensed band for short range communications where the oxygen absorption peak can be used to an advantage. Frequencies around the 94 GHz oxygen absorption minimum offer an opportunity to longer range. Possible W-band (75-110 GHz) use includes short to medium range high-speed communication links as well as radar, imaging and positioning applications.

Recently, fundamental mode CMOS oscillators have been reported up to 140 GHz [1] but with low power (-19 dBm). The highest output power in the 100 GHz range has been roughly −8 dBm (including probe loss) [2]. One of the disadvantages of advanced CMOS technology in analog context is the reduced power handling capability. Scaling of the device dimensions lowers maximum operating voltages which translates to lower output power. With this in mind we report a 100 GHz fixed-tuned CMOS push-push oscillator with higher output power (−3 dBm). Sufficient power is an advantage especially when used as local oscillator with passive mixers where the higher power can reduce buffering requirements. Frequency control was not included at this experimental stage.

II. Circuit Design

The oscillator circuit was fabricated in STMicroelectronics 90 nm bulk CMOS technology. This process is aimed at digital applications. Seven copper metal layers were available with the two topmost layers thicker than the others. Dedicated Metal-Insulator-Metal (MIM) capacitor processing was not used in this design since it is not available when striving for the best possible cost efficiency with a basic digital process option.

Before the circuit design phase, some of the circuit elements were characterized and optimized using test structures from earlier processing runs. Transistor layout and the details of the access geometry have a significant effect on the high frequency behavior of the device. In this case, we used an NMOS device with 80 parallel 1 µm wide fingers (total gate width 80 µm). Short gate fingers are required to minimize the gate resistance. Another important consideration is the parasitic gate-drain capacitance which also has a significant impact on the maximum oscillating frequency f_{max}. Our measurements indicate a transition frequency f_t of 130 GHz and f_{max} of approximately 180 GHz for the 80 µm device. BSIM3 model supplied by the foundry was used in the nonlinear simulations with added external parasitics to better match the measured behavior of the test devices. Similarly, test structures were made to characterize different passive structures. Loss properties of microstrip, coplanar waveguide (CPW) and grounded coplanar waveguide (GCPW) were compared but often the optimum choice depends on the function and characteristic impedance of the particular line. The ground plane in microstrip and GCPW should reduce coupling to the lossy silicon substrate. Mainly due to modeling and layout considerations, regular CPW was used for the oscillator design. Loss for a 50 ohm line is approx. 15 dB/cm ($\lambda = 2.3$ mm). Finger capacitors were used for DC-blocking and RF-shorts in the matching structures. By using stacked fingers with minimum line dimensions on the five thin metal layers capacitance density was found comparable to the optional MIM capacitors.

The circuit was realized in push-push configuration where the second harmonic signals from two oscillator structures are combined. The two structures oscillate with 180 degree phase shift. They are connected in such a way that the fundamental frequencies cancel each other at the output but even harmonics add in-phase (Fig. 1). The output network is designed so that node A in the diagram acts as a virtual ground for the fundamental signals. Parallel mode oscillation of the two structures has to be suppressed by ensuring that

oscillation start-up conditions are not fulfilled for one suboscillator with a load impedance $2 \cdot Z_{Load}$. Ideally, the load impedance does not affect the anti-parallel mode due to the virtual ground condition. The power output at signal frequency depends on the second harmonic content of the saturated waveform of the suboscillators.

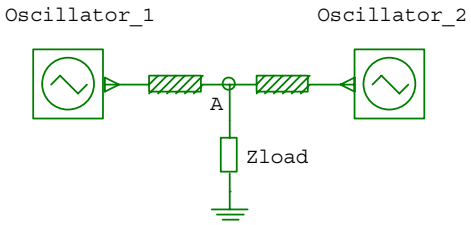

Fig. 1 Block diagram of a push-push oscillator.

The obvious advantage of the push-push approach is that higher frequency operation is possible since the needed fundamental oscillation is only at half the desired output frequency. Operating further away from the frequency limit of the transistor gives more freedom to select optimal device dimensions for e.g. power output or $1/f$ noise performance. With suitable buffering, the fundamental signal can also be extracted which makes phase locking in a VCO easier since frequency divider or down converter has to operate at only half the frequency. This can lower significantly the total power consumption in the phase lock loop. Furthermore, it is suggested that there is an advantages with respect to phase noise since the noise sources of the two suboscillators are uncorrelated but the signals add coherently [3]. This should give a 3 dB advantage over a fundamental oscillator and a doubler. In any case, higher resonator Q-values can generally be achieved at the lower frequency, and since the effect of the output load can be neglected for the fundamental signals, the loaded Q of a resonator increases even further with suitable circuit topology [4]. This decoupling of the output load for the fundamental frequency reduces also frequency pulling.

Since we had relatively good confidence in our transmission line models, these, instead of LC tanks, were used as resonators to avoid the need of inductor modeling and high quality capacitors. Initial analysis for each of the suboscillators can be made using ground connection at node A. A single transistor in common-gate configuration was used as a negative-resistance two-port for the oscillator core. Negative resistance generation was optimized by adding an inductive shorted transmission line on the gate. Drain and source ports were terminated with resonator impedances that fulfill the oscillation start-up conditions. Transistor drain and gate bias voltages are connected through low-impedance points in the resonator stubs (at RF short). The bias lines also include some filtering to suppress parasitic low-frequency oscillation modes. Highest power output was achieved by using the drain ports as output terminals. Tuning and optimization of the entire oscillator was done using harmonic balance in Agilent ADS. The simulated output power was –2.7 dBm at 100 GHz, single side band phase noise level –80 dBc/Hz at 1 MHz offset while the power consumption was 26 mW. Frequency control could be implemented by terminating the source resonator lines with varactors instead of open circuits. In the simulations this has negligible effect on power output or phase noise.

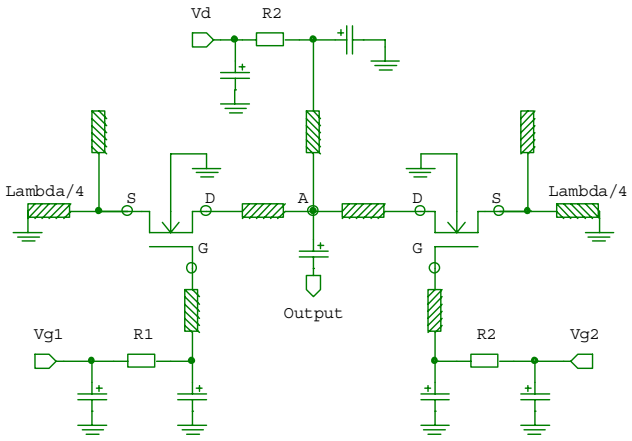

Fig. 2 Schematic of the 100 GHz oscillator.

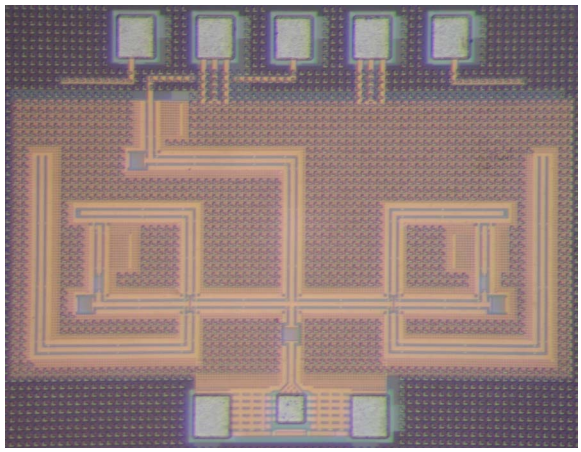

Fig. 3 Photograph of the oscillator. Chip dimensions are 1.1 x 0.8 μm^2.

III. Measurement Results

The oscillating frequency, output power and phase noise level were measured on-wafer using Agilent E4407B spectrum analyzer. An external harmonic mixer was used to downconvert the signal to the analyzer operating band. Fig. 4 shows the measured spectrum of the oscillator. The oscillating frequency is 101 GHz . To calculate the actual output power, the mixer conversion loss (39.5 dB) and wafer probe loss (1.5 dB) must be taken into account. The resulting output power is –3 dBm. Total power consumption of the two oscillator cores is 27 mW. This corresponds to 0.95 V drain bias voltage.

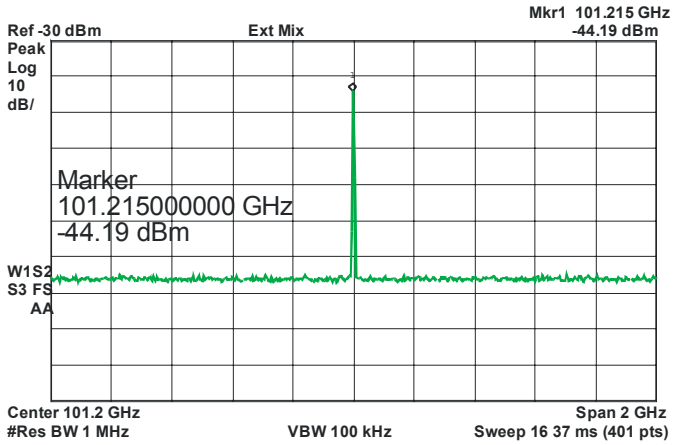

Fig. 4 Measured spectrum of the 100 GHz oscillator.

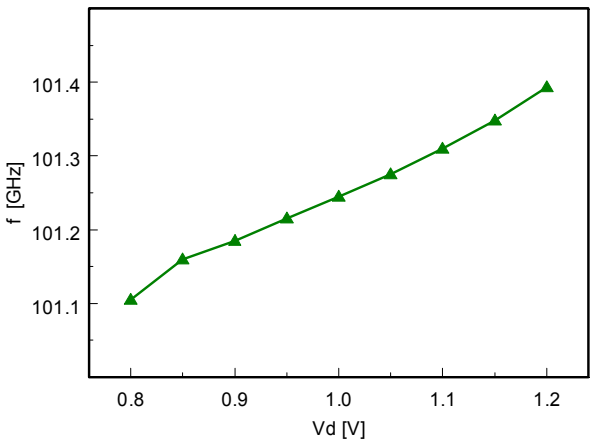

Fig. 6 Output frequency as a function of transistor drain voltage.

The SSB phase noise level is approximately −85 dBc/Hz at 1 MHz offset (see Fig. 5). Fundamental signal power at the output port was tested with a V-band wafer probing setup. The measured level was −58 dBm at 50.5 GHz which is 55 dB below the desired signal.

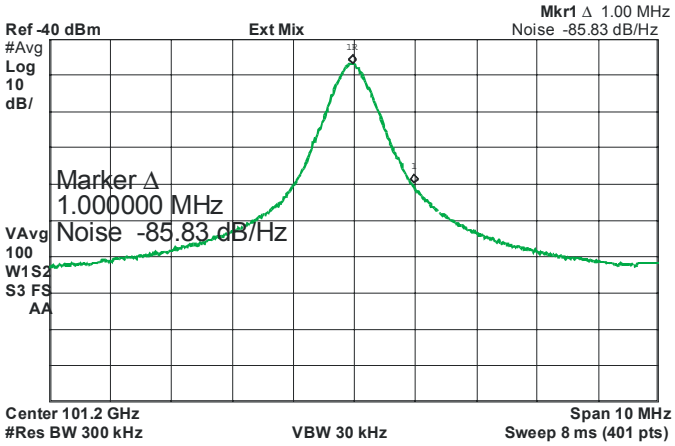

Fig. 5 Spectrum plot showing phase noise estimation.

Frequency push properties were also tested. Fig 6 shows the output frequency as a function of transistor drain voltage. Output power variation within the tested V_d range 0.8…1.2 V was -2…+0.2 dB.

IV. Conclusions

A 100 GHz CMOS oscillator was designed and measured using 90 nm bulk CMOS technology. The circuit is based on push-push principle and exhibits a relatively high output power of −3 dBm. The design is based on transmission line resonators. Consequently the phase noise is not particularly dependent on the quality of capacitors which enables the use of basic digital process option. The measured phase noise was −85 dBc/Hz and power consumption 27 mW. The measured performance corresponds very well to simulations. A drawback of the transmission line resonator approach even at this high a frequency is a larger chip area compared to LC tanks.

Acknowledgment

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References

[1] C. Cao and K. O, "A 140-GHz Fundamental Mode Voltage-Controlled Oscillator in 90 nm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, No. 10, pp. 555-557, Oct. 2006.

[2] B. Heydari, M. Bohsali, E. Adabi, A. Niknejad, "Low-power mm-Wave Components up to 104 GHz in 90 nm CMOS," *ISSCC Dig. Tech Papers, pp. 200-201, Feb. 2007.*

[3] R. Wanner, G. R. Olbrich, "A Hybrid Fabricated 40 GHz Low Phase Noise SiGe Push-Push Oscillator," *Topical meeting on Silicon Monolithic Integrated Circuits in RF Systems,* April 9-11, 2003, Garmisch, Germany, pp. 72-75, 2003.

[4] R. Wanner, R. Lachner, G. R. Olbrich, "A Monolithically Integrated 190 GHz SiGe Push-Push Oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 15, No. 12, pp. 862-864, Dec. 2005.

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