

26.1 A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna

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The uses of terahertz systems (300GHz to 3THz) in radars, remote sensing, advanced imaging, and bio-agent and chemical detection [1, 2] have been extensively studied. A compact and low-cost signal source is a key circuit block of terahertz systems. Traditionally, the circuits have been built using highly optimized III-V technologies [3, 4]. With the advances of CMOS, it has become realistic to consider terahertz circuits in CMOS. This paper reports a signal source operating near 410GHz that is fabricated using low-leakage transistors in a 6M 45nm digital CMOS technology.

The maximum oscillation frequency is limited by the unity maximum available power gain frequency, f_{max} of a transistor. To obtain even higher frequencies, the push-push oscillator architecture [5, 6] using the second harmonic has been used to generate a 192GHz signal in a 0.13 μ m CMOS technology [6]. Figure 26.1.1 shows a schematic of the push-push oscillator with a patch antenna. Presently, high frequency probes for measurements above 325GHz are not available. The on-chip patch antenna is used to extract the signal. Additionally, the parasitics of a package and interconnections between on-chip components and an external antenna impede signal transmission at terahertz frequencies. This causes signal attenuation and unwanted coupling. The use of on-chip antennas reduces loss and size as well as cost of systems.

Cross coupled transistors M_1 and M_2 form the oscillator core. Inductors L_1 and L_2 , and the capacitances of the cross-coupled pair determine the oscillation frequency. At the virtual ground nodes, the out-of-phase fundamental signals are attenuated, and the 2nd-harmonic is extracted and radiated through the on-chip patch antenna. In the push-push oscillator, the cross-coupled transistor pairs generate differential signals and eliminate the concern for even-mode oscillation. Quarter-wavelength transmission lines provide a high impedance at the 2nd-harmonic frequency. Two oscillators are implemented. The first oscillator includes buffers to measure the fundamental signal, while the second version does not include the buffers, which increases the output frequency. The fundamental oscillation frequency of the latter is ~16GHz higher than that of the oscillator with buffers. The buffers are tapered in order to lower the capacitive load in the oscillator core (Fig. 26.1.1). At 200GHz, since the low-leakage transistors do not have much gain, the buffer is expected to attenuate the signal. The primary role is to isolate the oscillator core from the 50 Ω load. The total bias current for buffers is 10mA.

For layout symmetry, the core is biased using two PMOS transistors through two quarter-wavelength transmission lines [6]. To have a higher operating frequency, varactors are not included. The transmission lines are formed using a grounded coplanar waveguide (GCPW) structure [7]. Compared to the conventional CPW, the insertion loss is lower because the ground plane isolates the line from the lossy silicon substrate. The lines are formed using the top metal layer with thickness of ~1.2 μ m, and the ground plane is formed using metal 1 and 2 layers. The characteristic impedance is 50 Ω and the length is 90 μ m. The separation between the signal and ground lines and between the signal and ground plane are ~4 μ m. The transmission lines and patch antennas are simulated using Ansoft HFSS.

The on-chip patch antenna consists of a patch and a ground plane as shown in Fig. 26.1.2 [8]. The ground plane once again shields the antenna from the lossy silicon substrate and makes the antenna characteristics to be less dependent on nearby metal structures. The ground plane also reduces the signal coupling from and to nearby circuits and metal lines. The patch length is about half

wavelength. The patch size is 200 \times 200 μ m² which is not excessively large. The aluminum pad layer is used to form the patch. The ground plane is formed by shunting metal 1 to 5 layers to lower the loss. The thickness of each metal layer is ~0.2 μ m. The separation between the patch and ground plane is ~4 μ m. The simulated directivity of the patch antenna is 5 and efficiency is 22%. The input resistance of the on-chip patch antenna is 50 Ω at 390GHz.

For fundamental output measurements, the buffer output node of the oscillator is connected to a GGB WR-5 (140 to 220GHz) waveguide probe. The fundamental output spectrum is measured using an OML M05HWD (140 to 220GHz) harmonic mixer and an Agilent E4448A spectrum analyzer. The conversion loss of the harmonic mixer is ~60dB. Figure 26.1.3 shows the measured spectrum of 189GHz fundamental signal. The output power after embedding the ~60dB harmonic mixer loss is about ~27dBm.

Detection of 400GHz signals is challenging. The output power of push-push oscillator decreases with frequency due to the decrease of transistor gain and increase of interconnection loss. The harmonics mixer loss also increases with frequency. More importantly, high-frequency probes as mentioned are not available at these frequencies. Because of these issues, optical techniques are utilized. The 410GHz 2nd-harmonic is measured using a Bruker 113V Fourier-transform infrared spectroscopy (FTIR) system. The FTIR system shown in Fig. 26.1.4 consists of a source, an interferometer, and a silicon bolometer. The oscillator is placed on the source position. A 5mil Mylar beam splitter is used to increase the sensitivity of interferometer at 400GHz. The scanning speed of interferometer has been changed to distinguish the noise of interferometer. Figure 26.1.5 shows the measured spectrum. The fundamental signal at 205GHz is also seen. For the absolute power measurement, the circuit is placed directly at the input of bolometer. Figure 26.1.6 shows the measured radiated power and operating frequency versus bias conditions. The supply voltage is 1.5V. As the current is increased, the oscillation frequency decreases, and the radiated power increases. The optical responsivity of silicon bolometer (HD-3, 1378) from Infrared Laboratories is 1.1 \times 10⁴V/W. At 11mA, the output frequency is ~410GHz and output power is ~20nW or ~47dBm. This low power is mostly due to the low gain of transistors and losses of thin metal and dielectric layers in the CMOS process, as well as the mismatch between the tuned frequencies of patch antenna and oscillator. The efficiency of the patch is in addition limited by the thin dielectric layer between the patch and its ground plane. In principle, the losses of metal lines and antenna efficiency can be drastically improved without significantly increasing the cost by using a back-end process better suited for terahertz applications. When the bias current is varied from 10 to 11mA, the frequency can be tuned by ~2GHz and the output power changes by ~3dB. Figure 26.1.7 shows the die micrographs of the two circuits. The chip area of circuits with buffers and without buffers is 350 \times 840 μ m² and 390 \times 640 μ m², respectively. Despite the low power, this circuit suggests the possibility of CMOS THz systems.

References:

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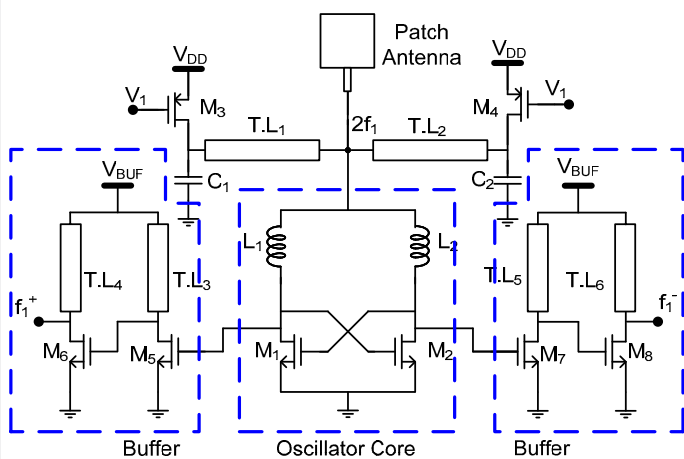


Figure 26.1.1: Schematic of push-push oscillator with an on-chip patch antenna.

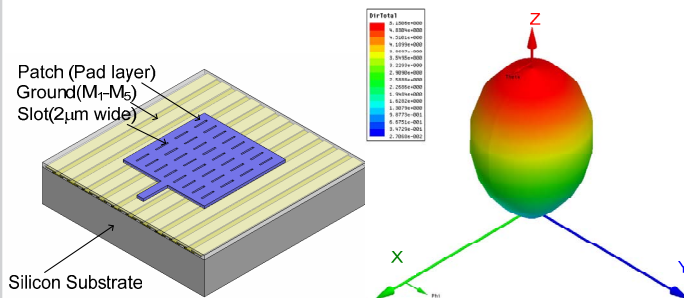


Figure 26.1.2: Patch antenna structure and HFSS simulated directivity.

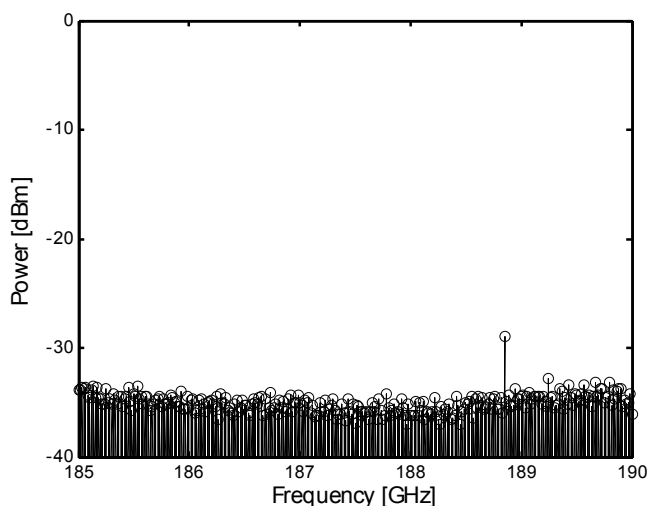


Figure 26.1.3: Power spectrum of the fundamental output measured using a harmonic mixer. The ~60dB loss of the harmonic mixer is de-embedded.

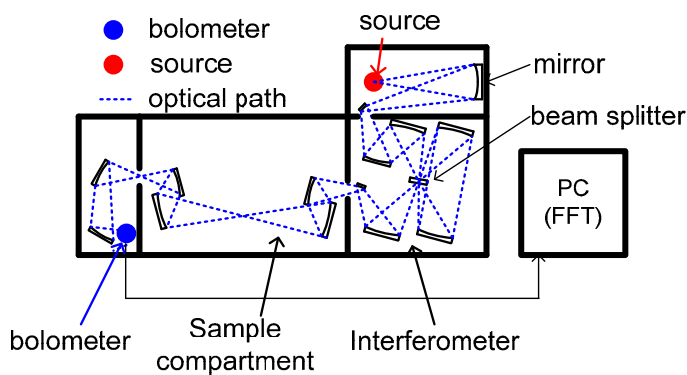


Figure 26.1.4: FTIR measurement setup.

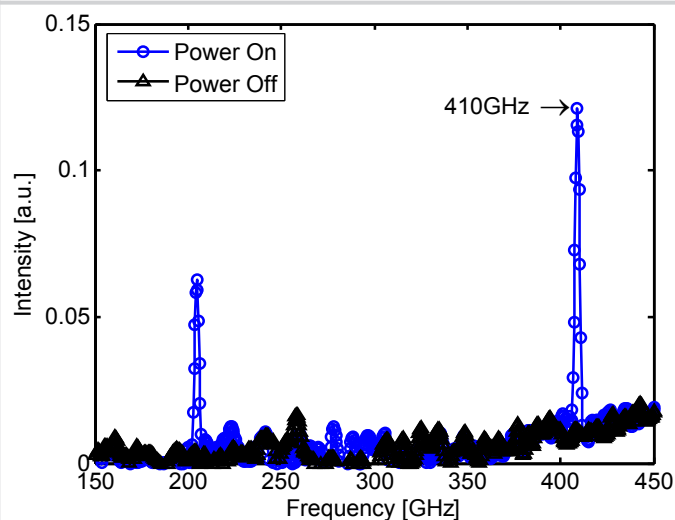


Figure 26.1.5: Spectrum of the push-push oscillator measured using a FTIR system.

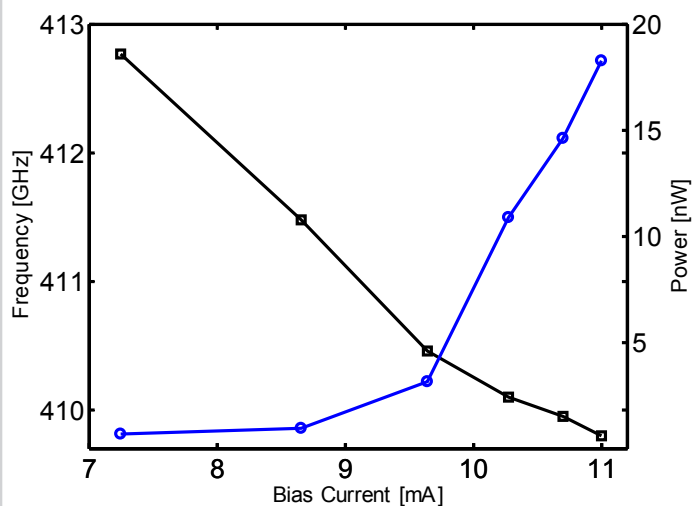


Figure 26.1.6: Output powers versus bias current measured using a bolometer.

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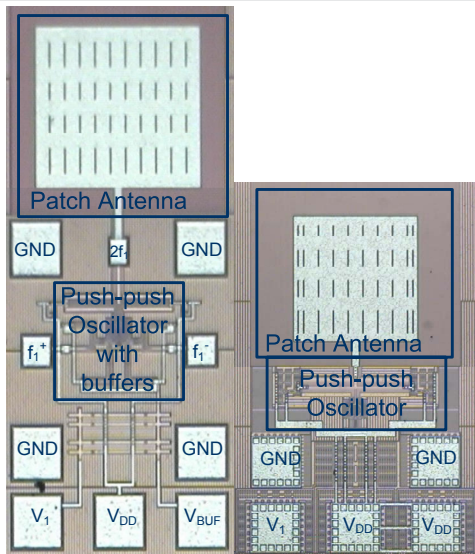


Figure 26.1.7: Die micrographs.