PLL & PLLVCO Serial Programming Interface (SPI) Mode Selection Design Considerations

Application Note

1 Table of Contents

Revision History

Revision	Date	Description
Rev 1.0	August, 2013	First release

2 Introduction

This application note discusses implementation details of the Serial Programming Interface (SPI) Mode selection feature of Hittite's PLL and PLLVCO product lines.

3 Applicable Products

This application note applies to the following products:

PLLs:
HMC703LP4E, HMC704LP4E

Narrowband & Triband RF PLLVCOs:
HMC820LP6CE, HMC821LP6CE, HMC822LP6CE, HMC824LP6CE, HMC826LP6CE, HMC828LP6CE, HMC831LP6CE, HMC836LP6CE, HMC837LP6CE, HMC838LP6CE, HMC839LP6CE, HMC840LP6CE

Wideband RF PLLVCOs:
HMC829LP6GE, HMC830LP6GE, HMC832LP6GE, HMC833LP6GE, HMC834LP6GE

Clock Generation:
HMC1032LP6GE, HMC1033LP6GE, HMC1034LP6GE

4 How does the Serial Interface (SPI) Mode selection work?

The devices covered in this document have two different serial interface modes: Open Mode and HMC Mode.

The serial interface mode selection occurs after power-up and is determined by the occurrence of either the SCK or SEN signal edge.

5 How to reliably select Serial Interface Mode

To reliably configure the device for the desired serial interface mode, the following power-up sequence must be used:

1. Apply power to the microcontroller/FPGA with the PLL or PLLVCO device unpowered;
2. Configure all the digital inputs (SEN, SCK, SDI, CEN) to be low. SDO should also be low;
3. Apply power to the PLL or PLLVCO device;
4. HMC Mode: Cycle SEN high then low. The rising edge on SEN will configure the device for HMC Mode;
   Open Mode: Cycle SCK high then low. The rising edge on SCK will configure the device for Open Mode;

If the wrong serial interface mode is entered, the only way to recover is to remove power from the device and follow the above procedure again.

6 How to reliably select Serial Interface Mode on multi-PLL or PLLVCO systems

In multi-device platforms that have more than one PLL or PLLVCO device and the intended serial interface mode is HMC Mode, it is critical that all devices be configured for the serial interface mode prior to writing/reading to/from any device.

If this is not done, the access to the first device will also apply SCK to the other non-accessed devices. This will force the non-accessed devices to enter Open Mode unless these devices have had a rising SEN edge applied prior to SCK.

In multi-device platforms that have more than one PLL or PLLVCO device and the intended serial interface mode is Open Mode, a write to any device will configure all devices for Open Mode because SCK is common to all devices, provided all SEN lines are held low until the first SCK edge occurs.

7 If digital signals cannot be held low prior to apply power to PLL or PLLVCO

In situations where the state of the digital signals from the microcontroller/FPGA cannot be held low prior to and during PLL or PLLVCO power-up, a couple of options are available.

1. Connect the Enable control of the regulator powering the PLL or PLLVCO device to the microcontroller/FPGA. On system power-up, have the microcontroller/FPGA disable the regulator until all the digital I/O signals are low. Then enable the regulator to apply power to the PLL or PLLVCO and follow the SPI mode setting directions above.

2. The microcontroller/FPGA should be programmed to operate in both HMC Mode and Open Mode. After power-up, a test is performed to determine which mode is active which the microcontroller/FPGA will then use. The test is simple:
   Program Reg0Fh = C0h: LD/SDO pin should go logic Low;
   Program Reg0FH = E0h: LD/SDO pin should go logic High;

If the output levels do not correspond to the expected level then the device is in the other SPI mode. Attempt the same exercise with the other SPI mode to confirm communication.

8 If SPI signals are toggling prior to application of power to PLL or PLLVCO

Voltages applied to device signal pins prior to the application of power can present a problem. ESD diodes inside an IC provide an undesired conduction path from signal pins through to power supply pins, as shown in Figure 1. When power to VDD has not been applied yet, the upper ESD diode can conduct. This has the unfortunate effect of providing a significant bias on the power pins, which can partially power-up the internal circuits.

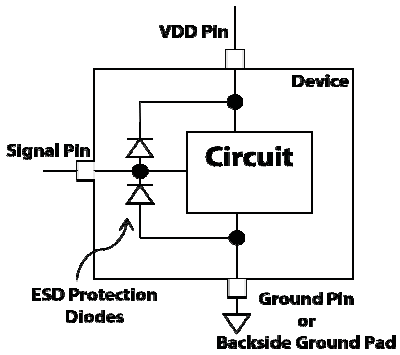

Figure 1 ESD Structure

One of the effects of this unwanted bias is that it can impair the function of the Power-On-Reset (POR) circuit. Figure 2 shows a simplified sketch of a POR circuit. The purpose of the POR circuit is to provide a delay at device power up until the power supplies are at a valid level and then resetting the digital circuits into a known state. This happens automatically every time the chip is powered up.

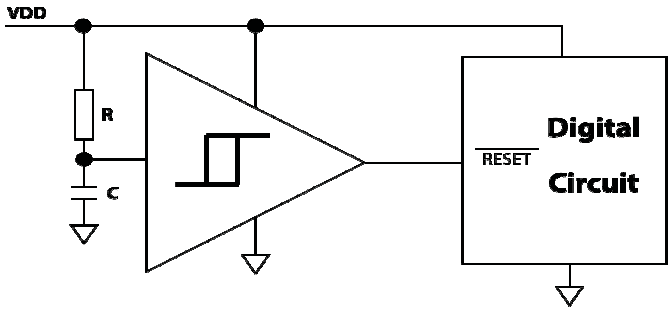

Figure 2 Simple POR Circuit

The time constant provided by the RC circuit delays the input voltage to the POR Schmidt trigger relative to the VDD voltage. This delay period has to be long enough to ensure the digital circuit is held in reset until the VDD voltage level is sufficiently high for the digital circuits to maintain their state. If the POR circuit removes the reset and goes high before a valid VDD exists, then the digital circuits may not maintain the desired reset state and could start in an unknown or illegal condition.

When signal voltages (and resulting path via the ESD diode to VDD) are present prior to applying VDD, then a partially charged RC chain inside the POR circuit may release reset early so that when VDD is applied, the digital circuits are not in the correct (reset) state. *One potential consequence is that the SPI Mode selection may not function* (SPI mode selection may already be set).

In summary, stray voltages or external logic signals should not be applied to the device prior to VDD. This includes voltages from logic devices on all pins, such as serial port pins or even external clock sources on reference input pins.

In the event such unintentional voltages are presented to the device, it is recommended that the microcontroller/FPGA be connected to the enable control of the regulator powering the PLL or PLLVCO. On system power-up, the microcontroller/FPGA should disable the regulator until all the digital I/O signals are low. After delaying, to allow the VDD to fully discharge, enable the regulator to apply power to the PLL or PLLVCO and follow the SPI mode setting directions above.