# TN06007

## V51RX2 Migration

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Technical note

Version 0.5

## 1. Introduction

This document provides information about the migration of the 89C51RX2 to the 89VRX2 in addition to the data sheet. It's good toknow the small differences between the two microcontrollers.

## 2. Differences between the C51RX2 and the V51RX2

The differences relevant for migration are mention in this tech note.

## 3. Pinning

The pinning of both micro's are the same.

## 4. Reset

The 89V51RX2 has a synchronous reset. The port pins will weakly pulled after oscillator startup by the internal reset algorithm. The 89C51RX2 however forces the port pins asynchronously to their reset condition when a voltage above Vil(min) is applied to the reset pin. The 89C51RX2 puts the port pins faster to their initial value than the 89V51RX2.

The program will starts 400msec @12Mhz after end of reset when no autobaud for entering ISP has been detected.

## 4. ALE pin

The ALE pin of the 89V51RX2 must have an update with a pullup resistor (between 3k and 50kohm) in those applications where the load capacitance is larger than 30 pF during reset. Otherwise the micro might enter a test mode.

## 5. EAn pin

The EAn pin of the 89V51RX2 is 12 volt tolerant.

## 6. ISP mode

The 89V51RX2 does enter the ISP mode when autobaud character has been detected within 400 msec @12Mhz

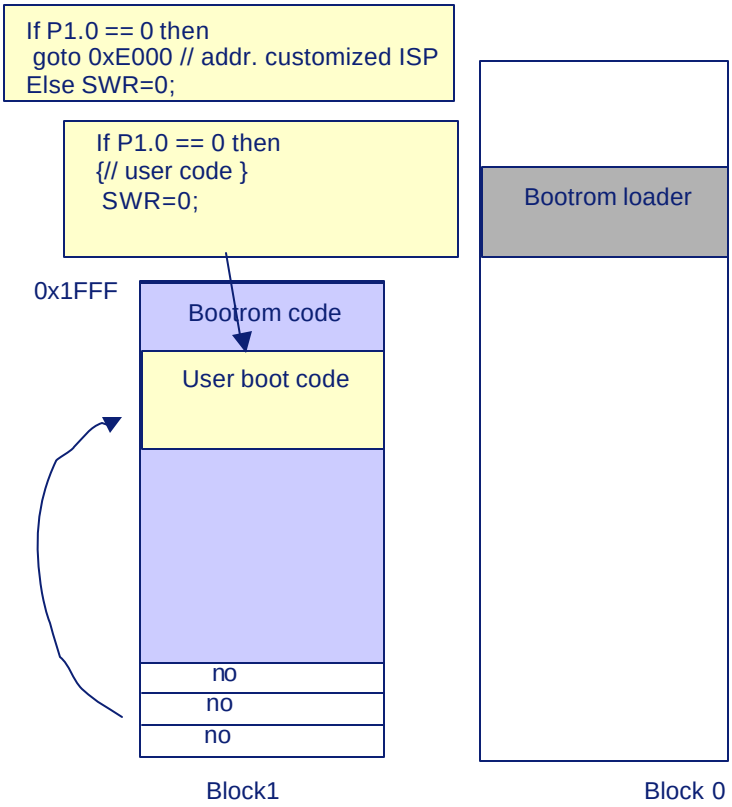
Setting the oscillator frequency is not necessary. The 89V51RX2 does respond to a "Specify Oscillator Frequency" string with a "."

The P89V51RX2 has the possibility to erase page of 128 bytes and to erase program the 6x/12x mode bit. After a reset the new mode is active. The ISP version, programmed in the P89V51RX2, can be read .

The "erase block mode" command of the 89C51RX2 will erase the total user memory. Application program should be modified to "erase page' command when this command is in use.

The 89V51 RX2 does not have a vector address mechanism like the 89C51Rx2. Customers who have their own boot routine have to update the bootrom of the P89V51RX2. If the size of the customized ISP routine is small the program can be located in block 1. Otherwise only a jump to an address in block 0 (above address 0x1FFF) has to be programmed in block 1. After clearing bit SWR (SoftWare Reset) the micro will start at address 0 of block 0. The example uses P1.0 for switching to (customized) ISP routine. The code in block 1

must be located between 0x500 and 0x1E00. Check always the hex files if these locations are free. Do not use the locations above 0x1E00. This is in use for data storage.




- Download latest version of bootrom code (hex file) from the web
- Download bootrom loader for programming block 1

- Implement ljmp to User code program in hex file
- Make user code

- Load bootrom loader in block 0
- Run bootrom loader and start Flash Magic
-
- Load/program bootrom code and usercode

## 7. IAP mode

The table shows the differences between the two micro's. The application program has to be modified to the new IAP entry point and the new boot enable control bit location (FCF.0). For compatibility of watchdog the reset bit FCF.1 (SWR) should be "0" when watchdog is active.

| Description | 89C51RX2 | 89V51RX2 | Remark |
|---|---|---|---|
| Boot block | 0xE000-0xFFFF | 0- 0x1FFF | |
| Boot enable bit | AUXR1.5 (enboot) | FCF.0 (BSEL) | |
| IAP entry address | 0xFF00 | 0x1F00 | |
| | | | |

Setting the oscillator frequency is not necessary. The 89V51RX2 does not use the information of R0 register anymore.

The 89V51RX2 has the possibility to erase page of 128 bytes and to erase program the 6x/12x mode bit. After a reset the 6x/12x mode becomes active.

The "erase block mode" command of the 89V51RX2 will erase the total user memory. Application program should be modified to one or more "erase page' commands when this command is in use.

## 8. Clock control

The peripherals (Watchdog,PCA,UART,Timers0,1,2) of the 89V51RX2 cannot run on in "12 clock mode" while the CPU is running in "6 clock" mode. When the application does use this feature of the 89C51RX2 the counter and baudrate reload values have to be recalculated for the "6 clock" mode.

The control bit for switching from 6x/12x mode for the 89V51RX2 is located in register FST.3 instead of CKCON.0 for the 89C51Rx2. The application software needs to be updated.

## 9. Watchdog

The watchdog timer differs from the watchdog timer of the 89C51Rx2. The software has to be rewritten.

The control register WDTC (0xC0) has an other address and a reload counter value has to be defined in register WDTD (0x85). Also the control differs from the 89C51RX2. Below you find a code example for the P89V51Rx2.

```
Init:
    {
    WDTD= reload value ; // Reload value counter for specific period .See data sheet
    WDTC= 0x31;    // 00011001 = output enabled, watchdog timer reset enabled, Start timer.
   }
Main:
    {
     While 1;
    {
        WDTC |= 0x02; // reset Watchdog counter
         // user program
       }
```

## 10. Parallel programming

The 89V51RX2 cannot be programmed with the same algorithm as the 89C51RX2. Please contact the programmer manufacturer for an update.

## 11. Security

The 89V51RX2 does have one security bit. When programmed no MOVC instruction can be executed from external memory to fetch code from internal memory .EAn is latched on reset and further programming of the flash is not possible. Verify is also disabled. Code in block 1 may program block 0 and vice versa. This is the same level of security as a 89C51RX2 with all security bits programmed.

## 12. Power consumption

TA= -40C to +85C;Vdd 4.5-5.5V

| I supply | Unit | P89C51RX2 | | | P89V51RX2 | | |
|---|---|---|---|---|---|---|---|
| Active | | min | typ | max | min | typ | max |
| @12Mhz | mA | | | 30 | | | 23 |
| @33Mhz | mA | | | 49.7 | | | |
| @40Mhz | mA | | | 56 | | | 50 |
| | | | | | | | |
| Idle | | | | | | | |
| @12Mhz | mA | | | 11.8 | | | 20 |
| @33Mhz | mA | | | 12.5 | | | |
| @40Mhz | mA | | | 15 | | | 42 |
| | | | | | | | |
| Powerdown | | | | | | | |
| | uA | | | 50 | | | 90 |
| | | | | | | | |
| IAP | | | | | | | |
| @12Mhz | mA | | 59 | | | | 70 |
| @33Mhz | mA | | 89 | | | | |
| @40Mhz | mA | | 99 | | | | 88 |

## 13. Hardware

Old applications with minimum decoupling might need an update for migration to the 89V51RX2. In general no problem are expected. A check on waveform of the Vdd of the micro is advisable.

## 14. Emulation

The P89V51RX2 does support the enhanced hooks emulation instead of the hooks emulation like the P89C51RX2. Contact your emulation manufacturer for the possibilities to update the emulation system. In practice the existing emulation system of the P89C51RX2 can be used.

## 15. Remark(s)

1. Within a short notice a new release of the ISP/IAP software which emulates the C family ISP/IAP . The customer can download and update the software in the field.

## 16. References

a. Info Product line

b. Data sheet